

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory, CPU-PEG/Display	3,4
CPU-Control/MISC/CFG/Audio	5
CPU-Power,CPU-GND	6,7
DDR4 1/2,DDR4-POWER/GND-1/2	8,9,10,11
PCH-USB/PCIE/DMI/SATA	12
PCH-Audio/Display/Clock	13
PCH-GPIO/USBOC#/SATASTRAP	14
PCH-LPC/SPI/SMBUS/MISC	15
PCH-Power,PCH-GND,PCH-Strap	16,17,18
PCIE SLOT-CPU(X16)	19
PCIE SLOT-PCH(X1)	20
SIO-NCT5563D-M/FAN CONTROLLOR	21,22
AUDIO - ALC892/887,AUDIO - depop circuit	23,24
LAN - RTL8111H	25
DVI/HDMI/VGA	26,27,28
USB2.0/USB3.0/SATA connector	29,30,31
CUT_VBAT circuit/BIOS ROM	32,33
ACPI CONTROLLER	34
PWM-RT3606BC/VCORE 3PHASE/VGT 2PHASE	35,36,37
DDR-RT8231/DDR-MP2147-VPP25	38,39
CPU PWR_ST/PLL	40
PCH Core power	41
VCCSA - POWER/VCCIO - POWER	42,43
ATX F_Panel/TPM/MSI_LED	44
DEBUG LED/EMI CAP/Manial Part	45,46,47
Power Map/Power Sequence/GPIO MAP	48,49,50
Revision History	51

MS-7996

ATX:235*180

Ver: 12

Intel -SkyLake-S plamform

CPU:

LGA1151

CPU POWER PAK *3 Phase

GT POWER PAK *2 Phase

System Chipset:

SPT-H :B150

SPT-H :H150

Onboard Chip:

HD Audio Codec: ALC892

SIO: NCT5563D

Flash ROM: SPI 64 MB

DP to VGA: ITE6515

PWM:

VCORE - RT3606

DDR - RT8231

PCH(1.0V) - UP1540

VCCSA - RT8125C

VCCIO - NB681(Converter)

VPP25 - MP2147

Main Memory:

DDR4 * 2 (Dual Channel)

LDO:

VCCSTPLL - GS7133

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501


3VSB:GS7133+PN MOS

3VDSW:GS7133

Expansion Slots:

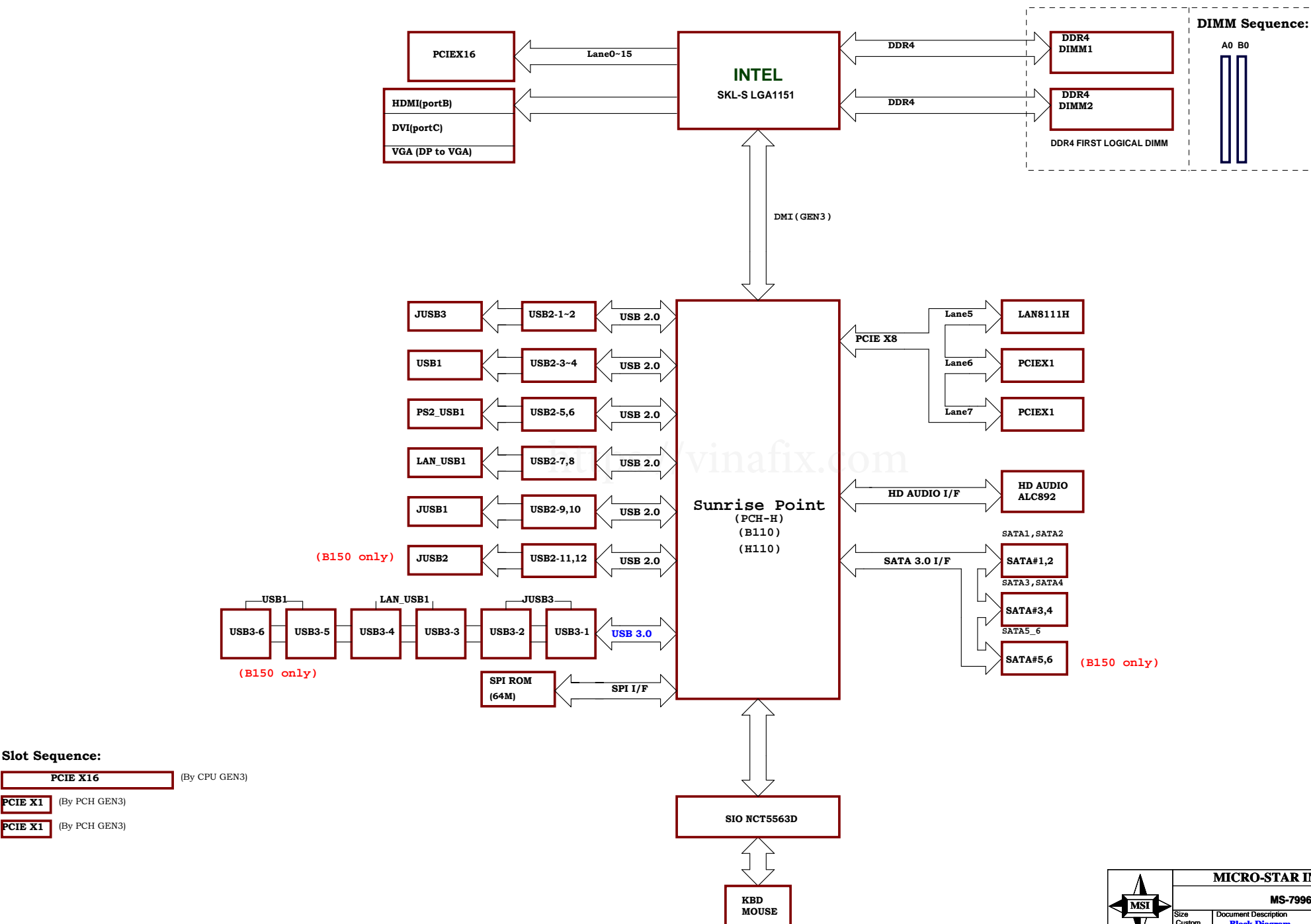
PCI Express (X16) Slot * 1

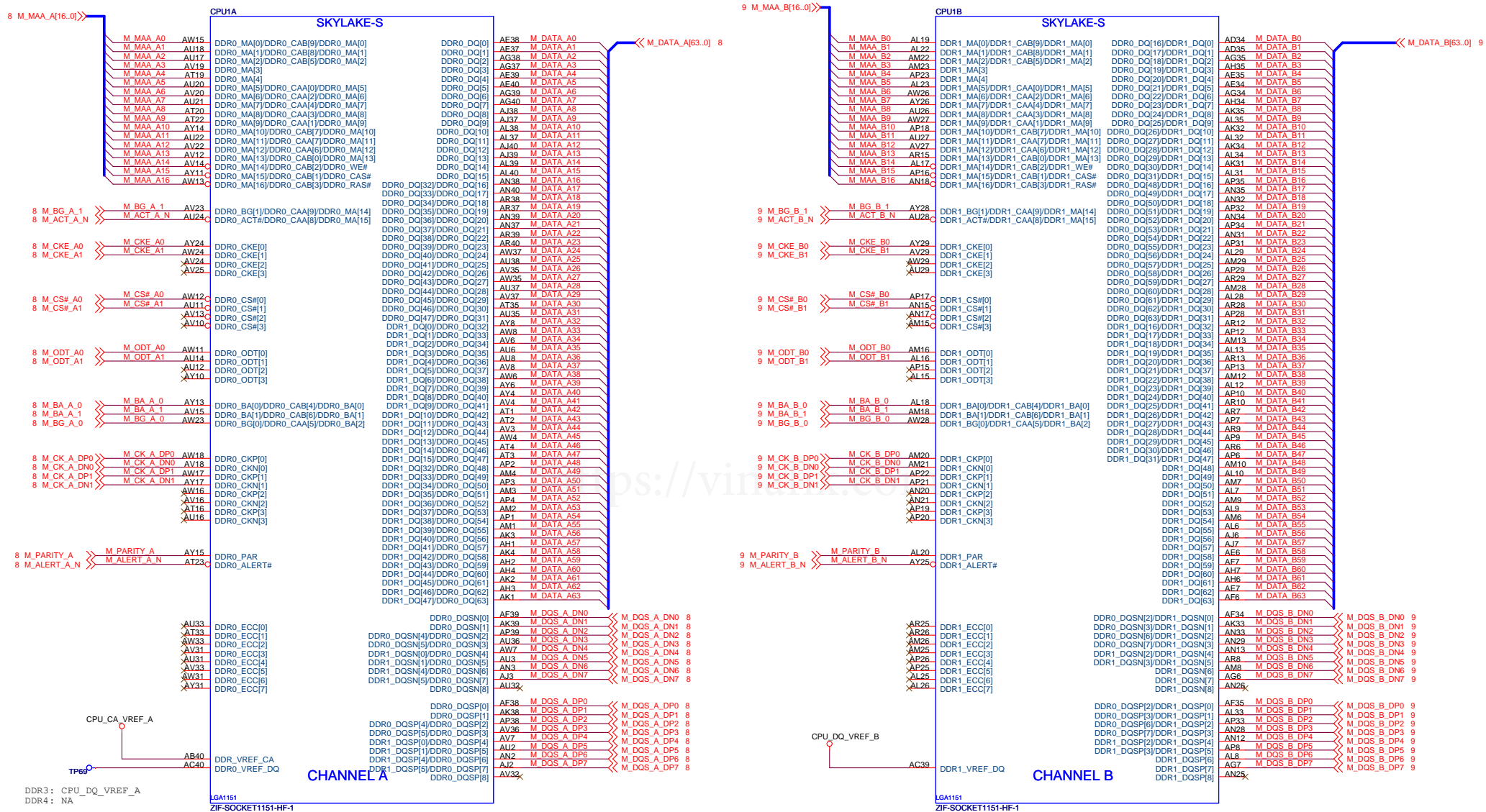
PCI Express (X1) Slot * 2



MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description Cover Sheet	Rev 12
Date: Wednesday, September 23, 2015		
Sheet 1 of		51

MS-7996 Block Diagram





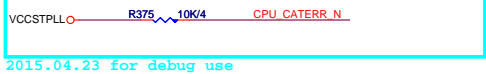
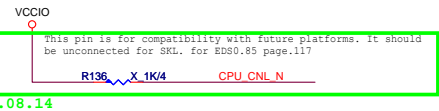
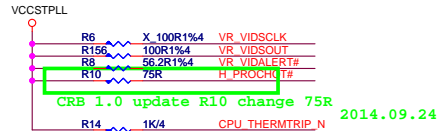
See Page11 circuit



MICRO-STAR INT'L CO.,LTD

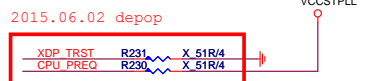
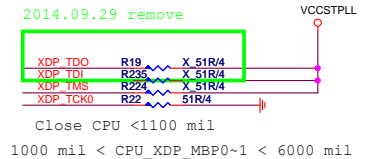
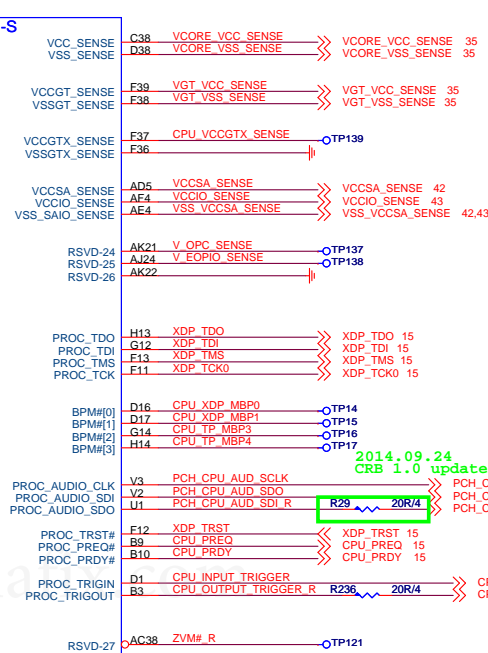
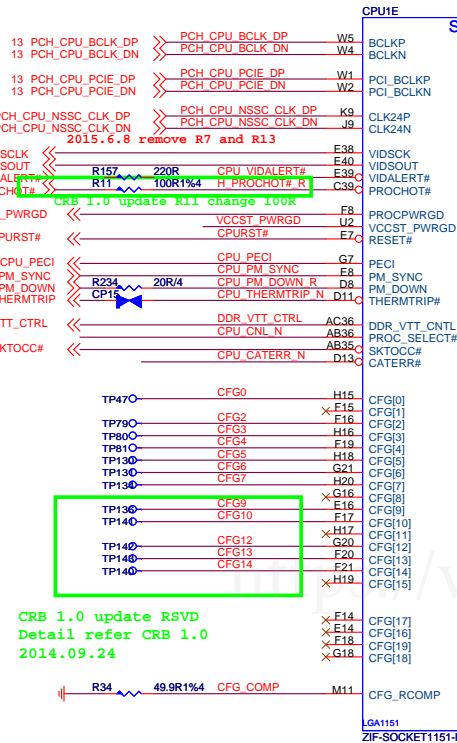
MS-7996

Size Custom	Document Description CPU-Memory	Rev 12
Date: Wednesday, September 23, 2015		Sheet 3 of 51

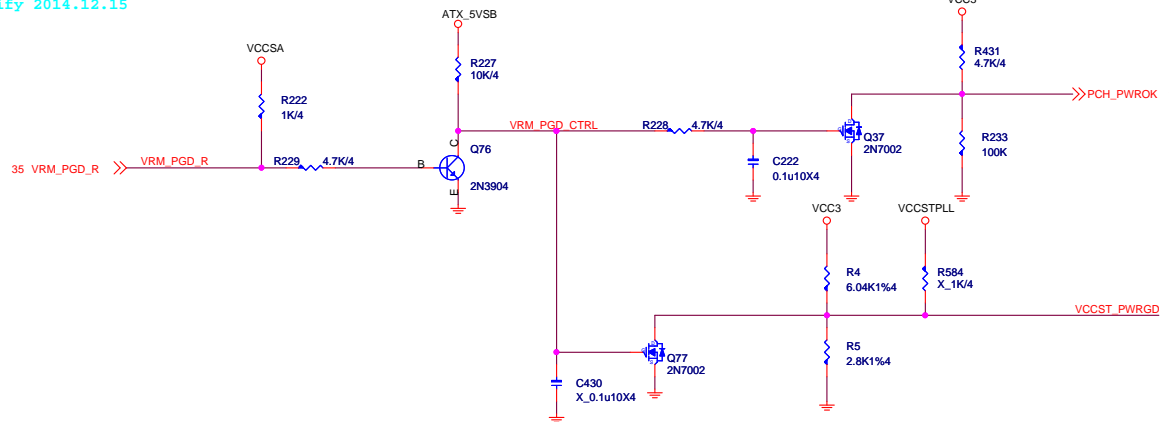


CFG Strap

CFG Table			
HIGH	LOW	DESCRIPTION	
0	No Lock	Lock	PCU PLL lock
1		RSVD	
2	NORM	REVERSE	PEG LANE REVERSAL
3		RSVD	
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL(0)
6	DISABLE	ENABLE	PEG0CFGSEL(1)
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8		RSVD	
9		RSVD	
10		RSVD	
11		RSVD	
12		RSVD	
13		RSVD	
14	RSVD		
15	RSVD		

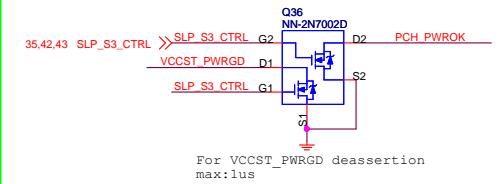


modify 2014.12.15



modify 2014.09.19

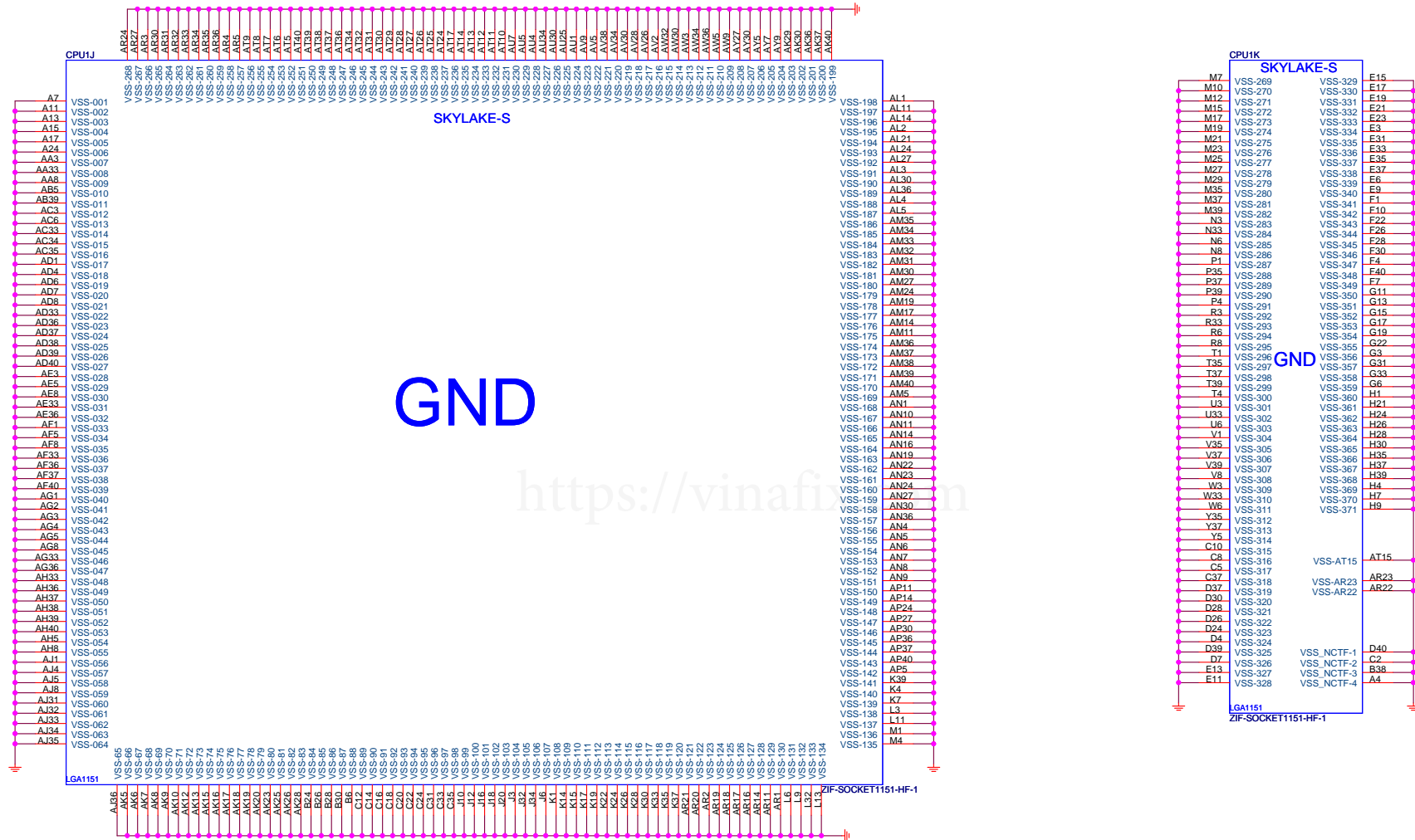
POWER DOWN

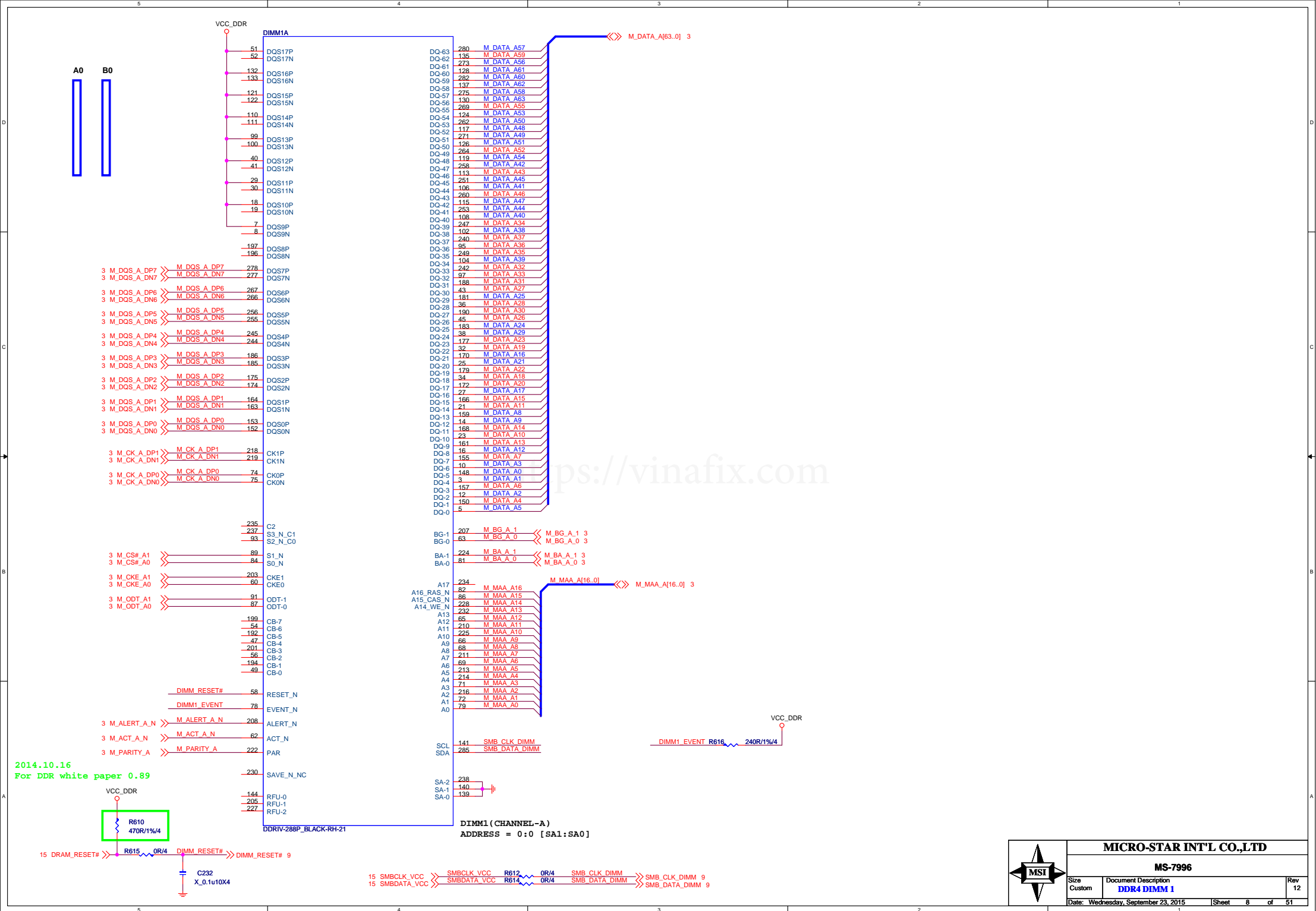


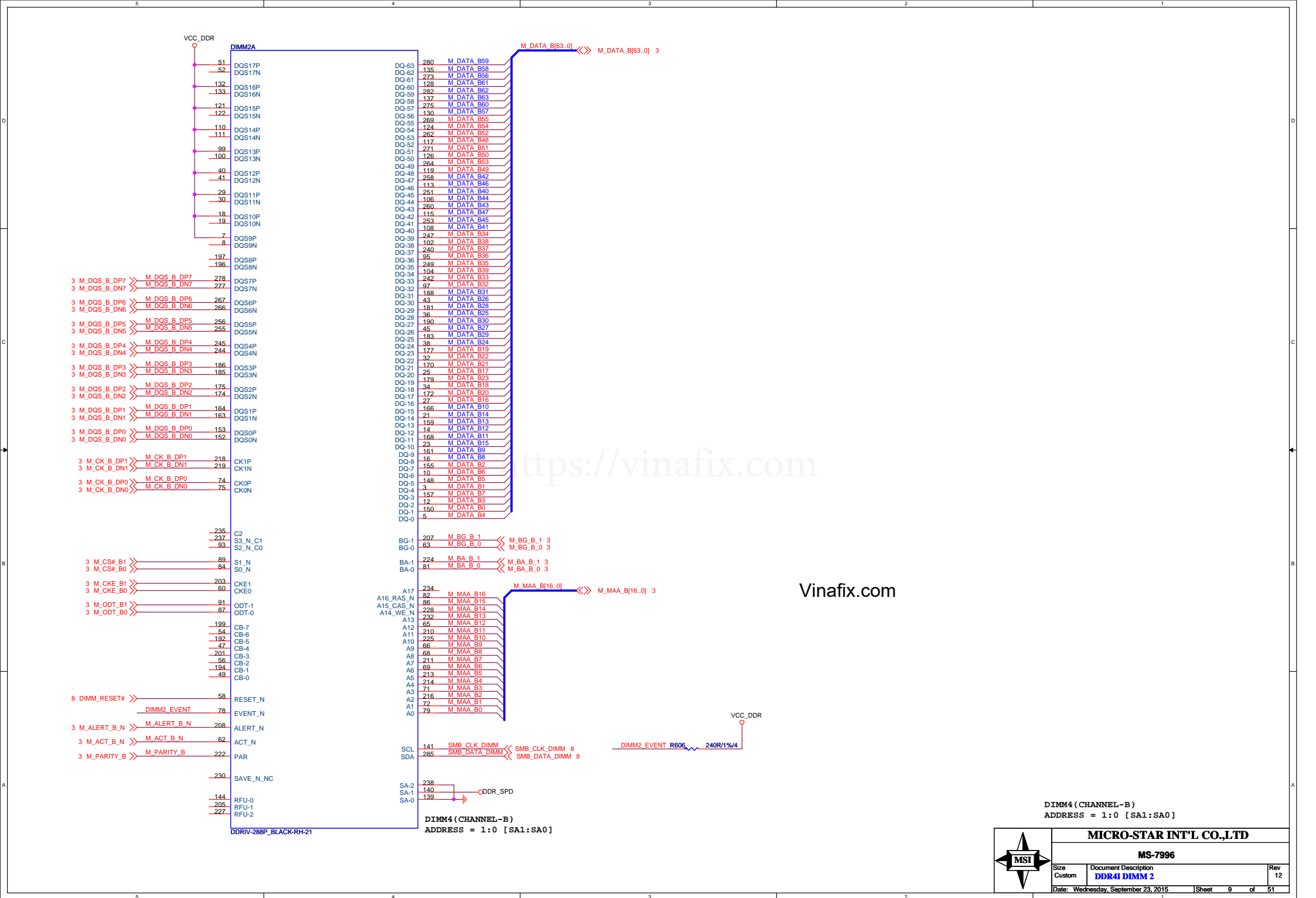
MICRO-STAR INT'L CO.,LTD


MS-7996

Size	Document Description	Rev
Custom	CPU-Control/MISC/CFG/Audio	12
Date:	Wednesday, September 23, 2015	Sheet 5 of 51









DIMM4 (CHANNEL-B)

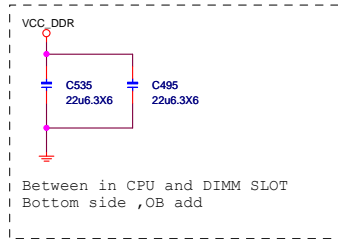
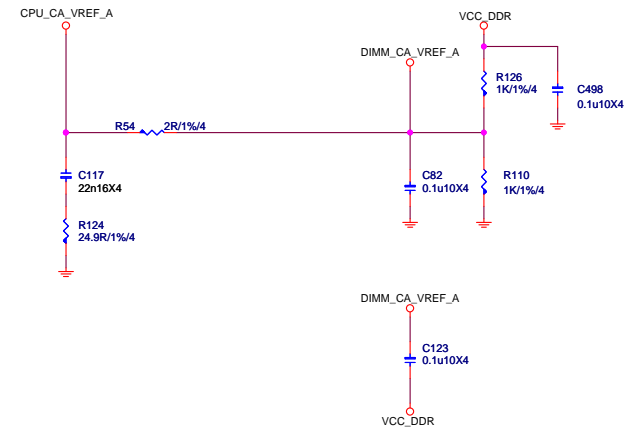
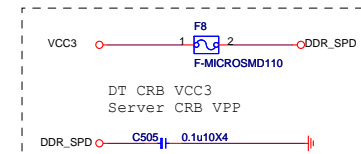
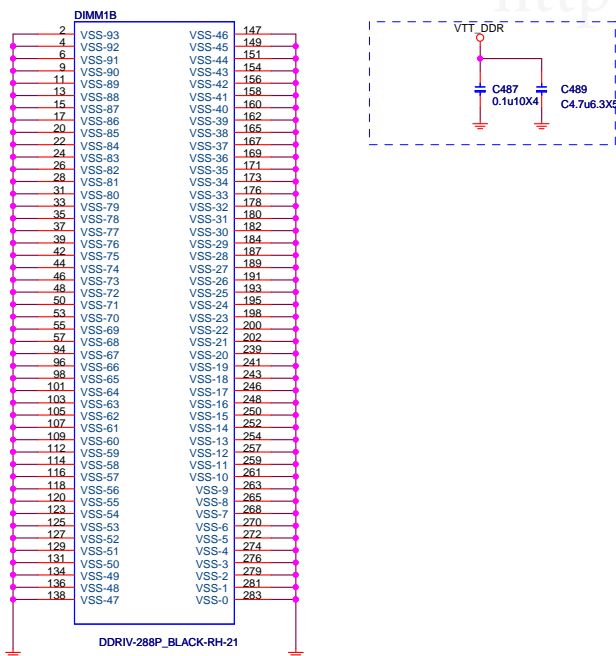
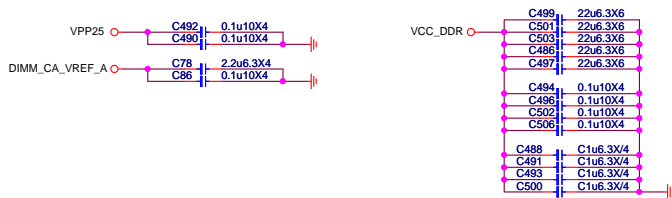
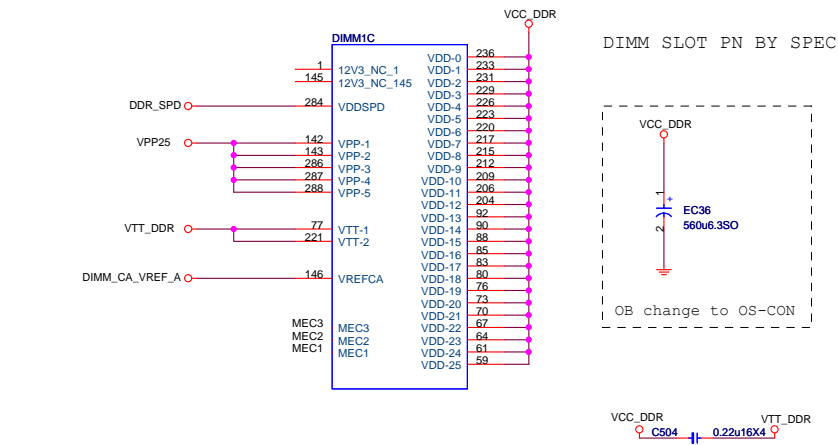
ADDRESS = 1:0 [SA1:SA0]

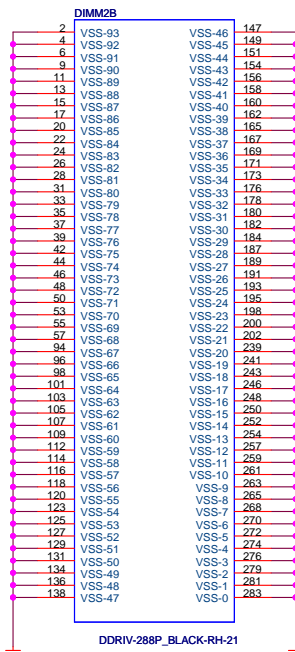
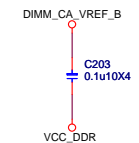
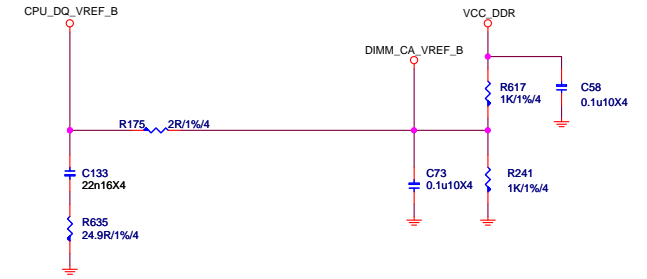
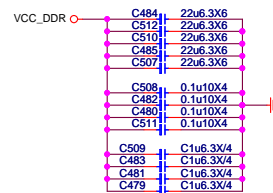
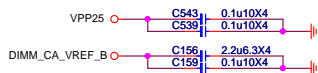
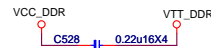
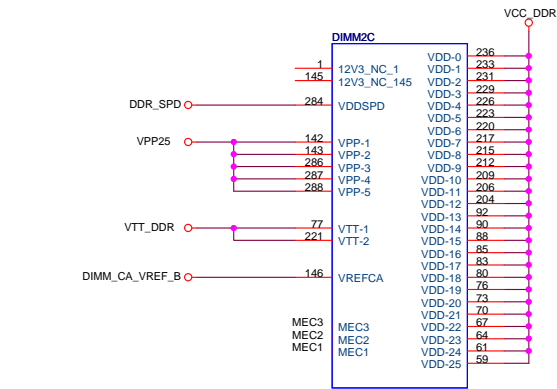
MICRO-STAR INT'L CO.,LTD

MS-7996

Size	Document Description	Rev
Custom	DDR4 DIMM 2	12

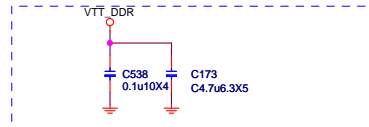
Date: Wednesday, September 23, 2015Sheet 9 of 51

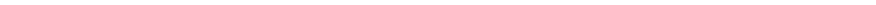
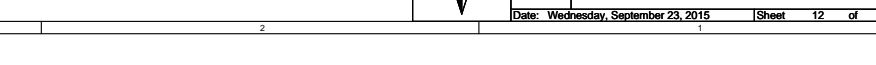
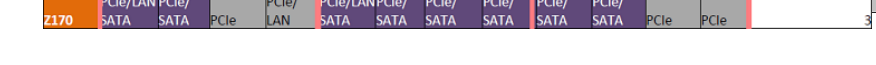
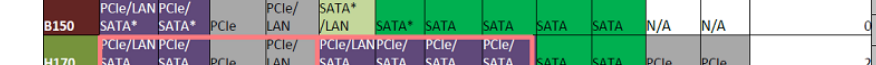
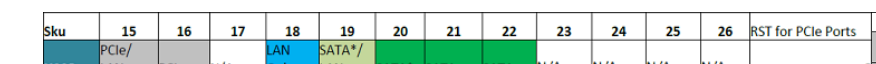
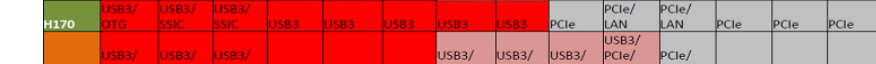
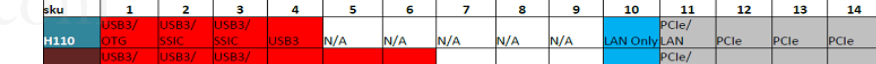
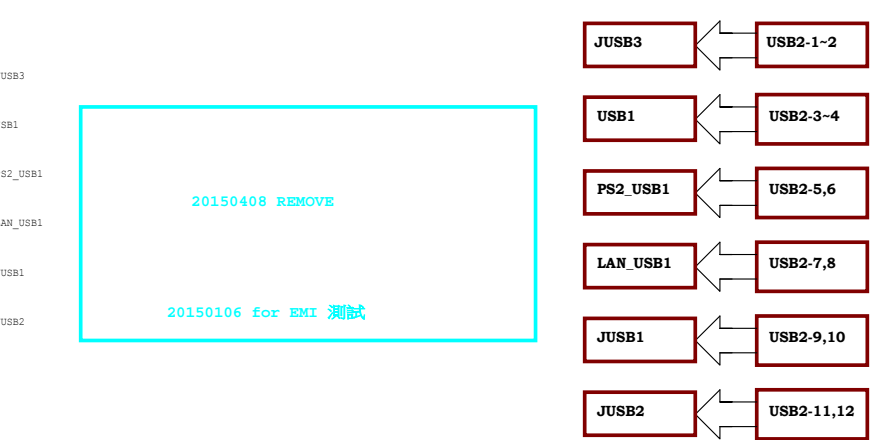
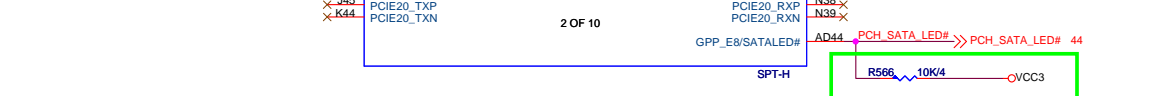
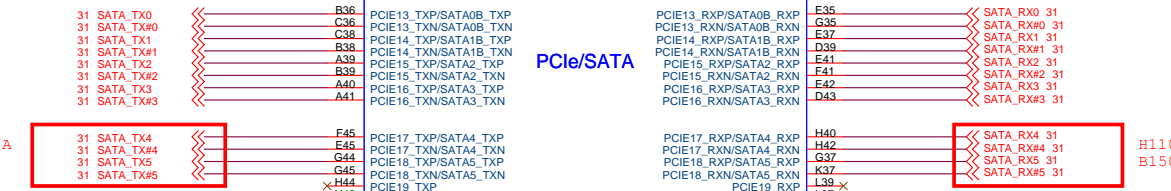
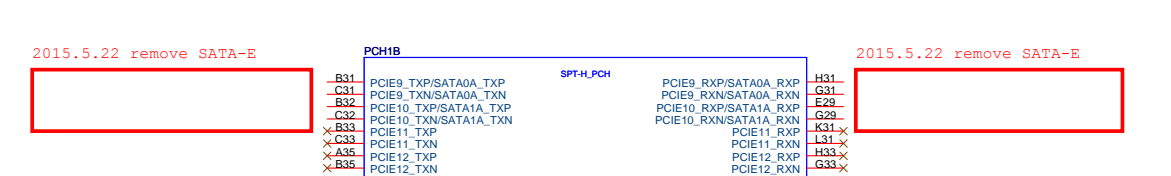
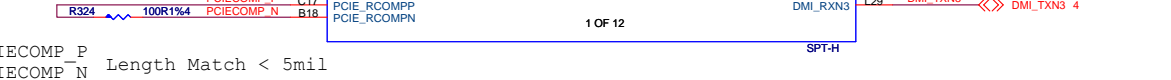
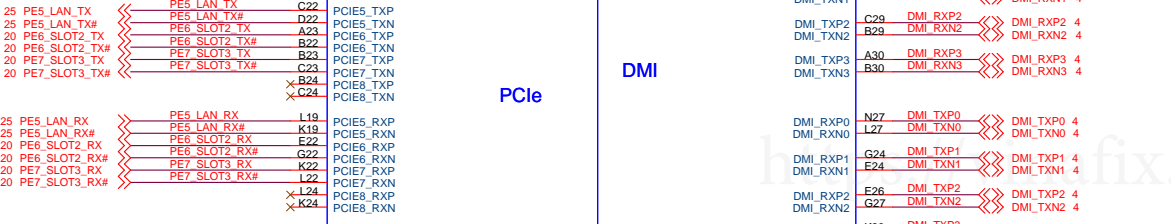
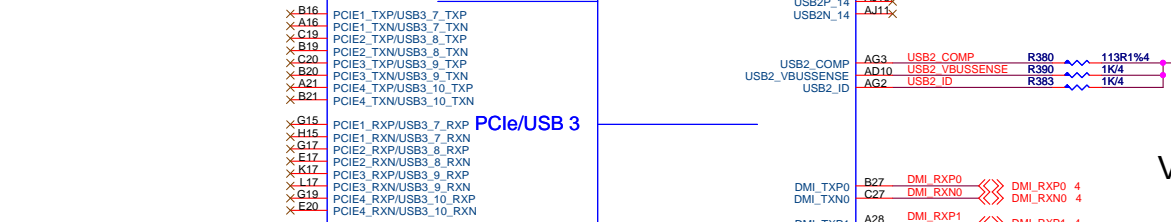
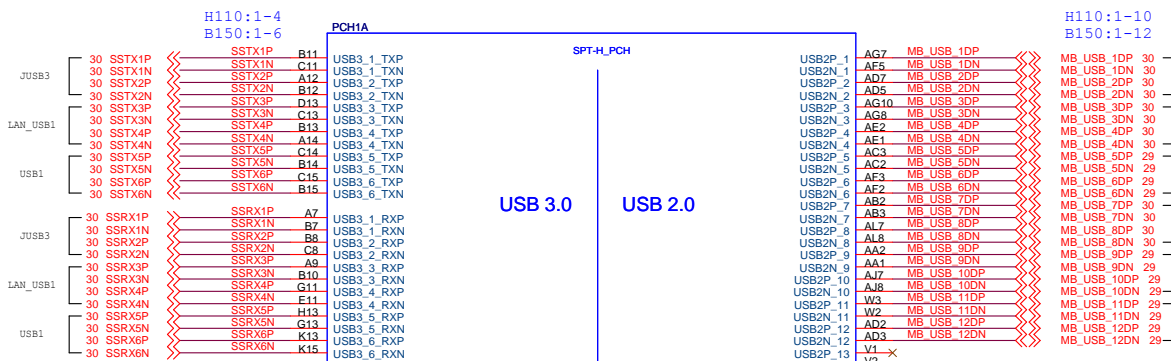


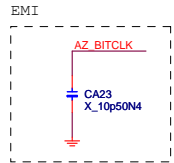


<https://vinafix.com>

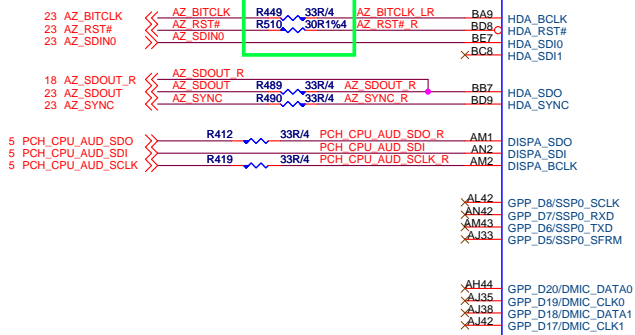
0.1uFxl per dimm







2015.7.28 R510 33R--30R



AUDIO

GPP_I[3:0] with SMI/NMI

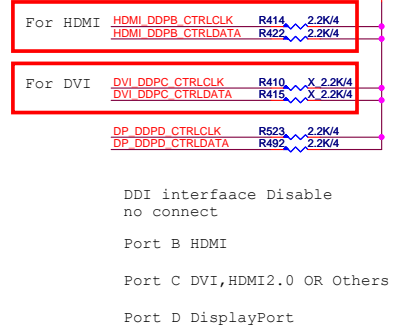
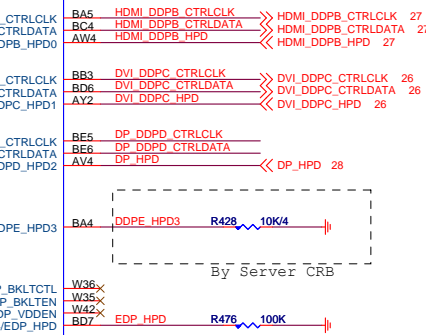
Port B

Port C

Port D

eDP

4 OF 10



DDI interface Disable
no connect

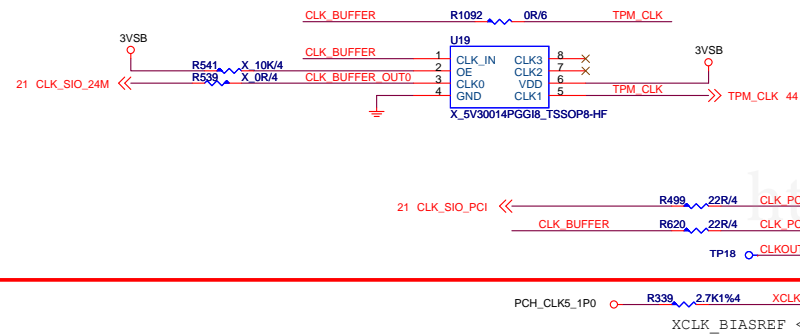
Port B HDMI

Port C DVI,HDMI2.0 OR Others

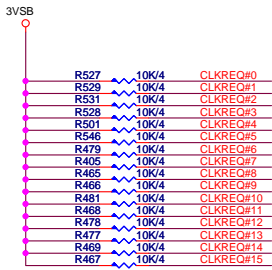
Port D DisplayPort

2015.6.1 updata circuit

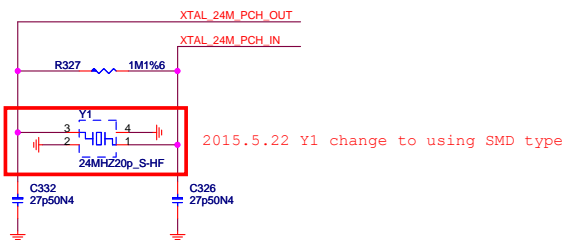
24M CLOCK BUFFER



Clock



Connect to SLOT Pin B12
for support L1 PM Substates
MS also can disable this function.



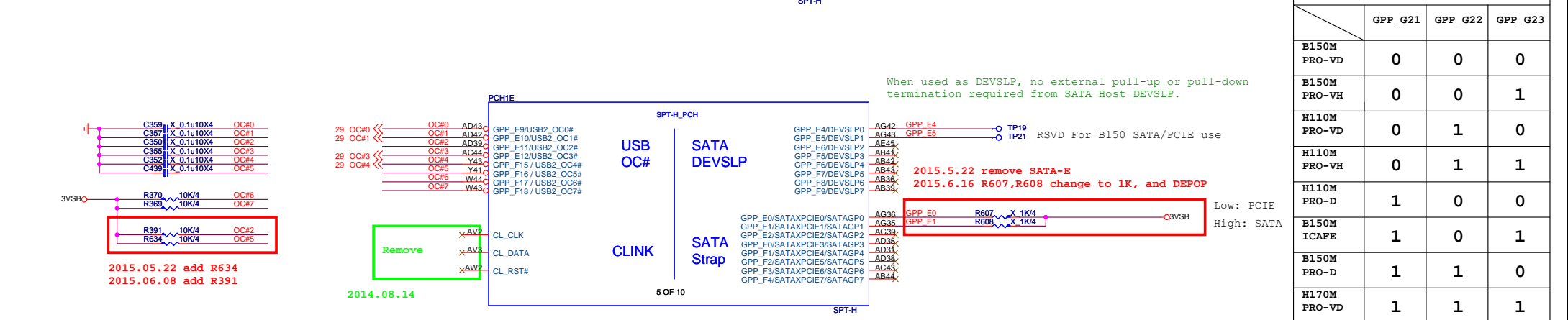
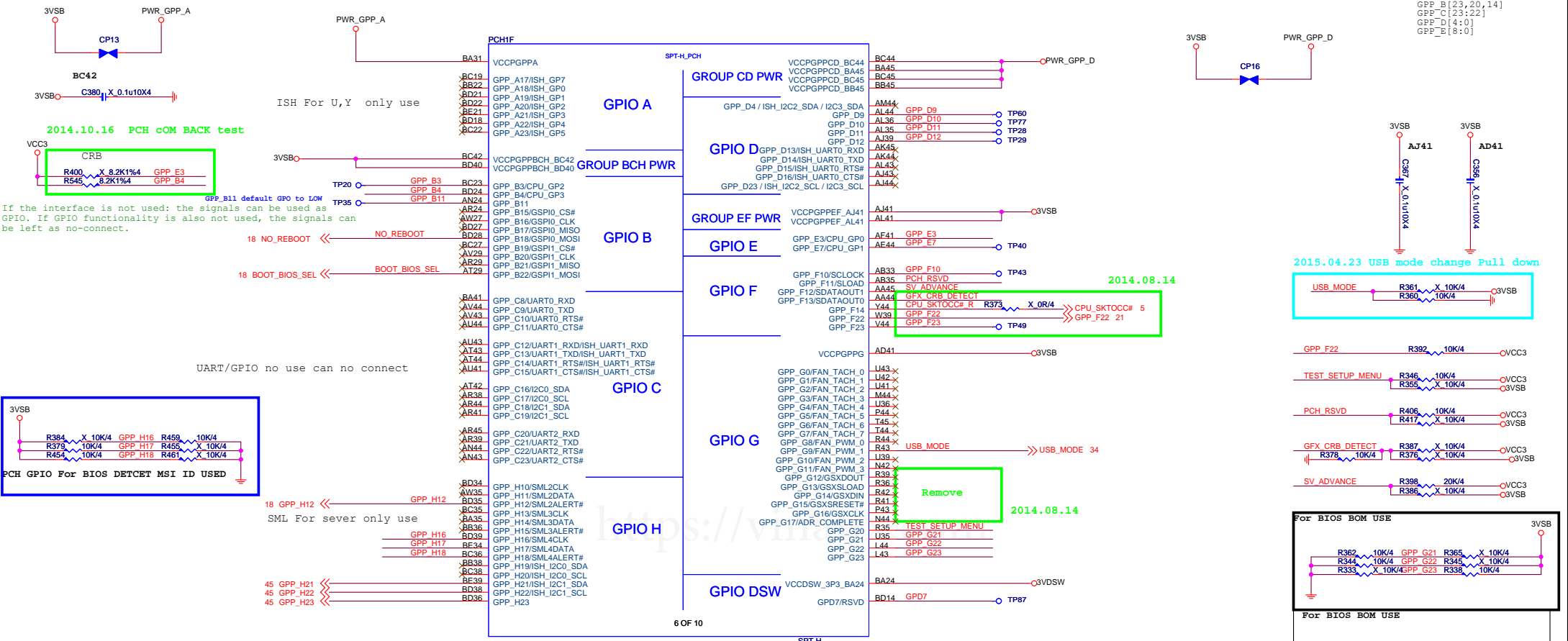
2015.5.22 Y1 change to using SMD type

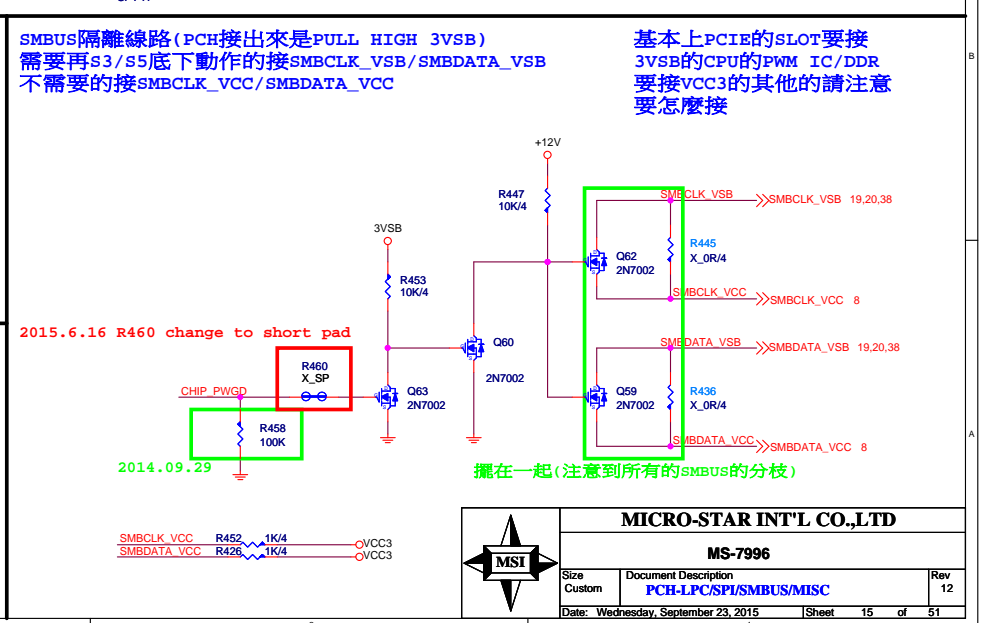
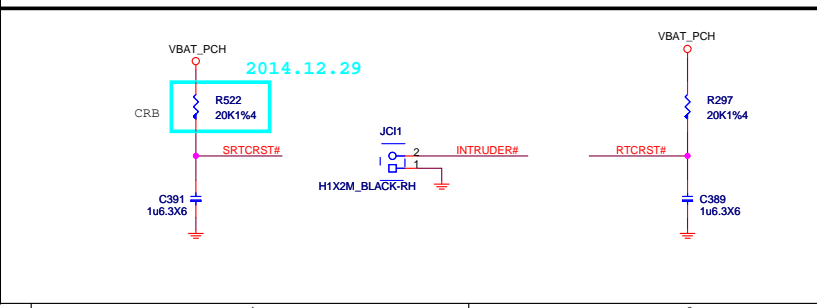
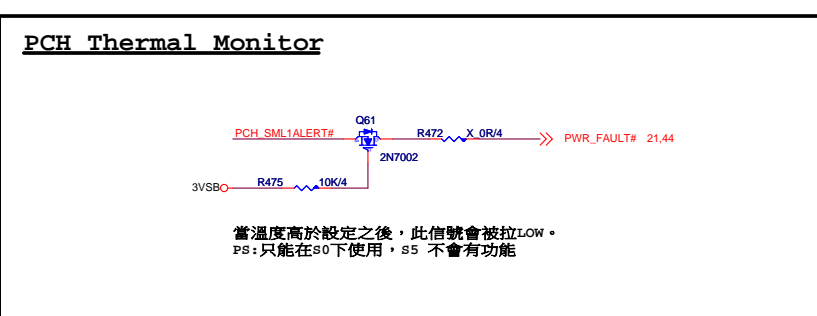
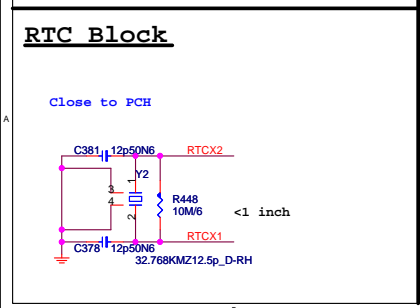
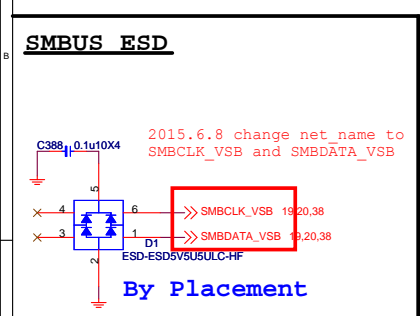
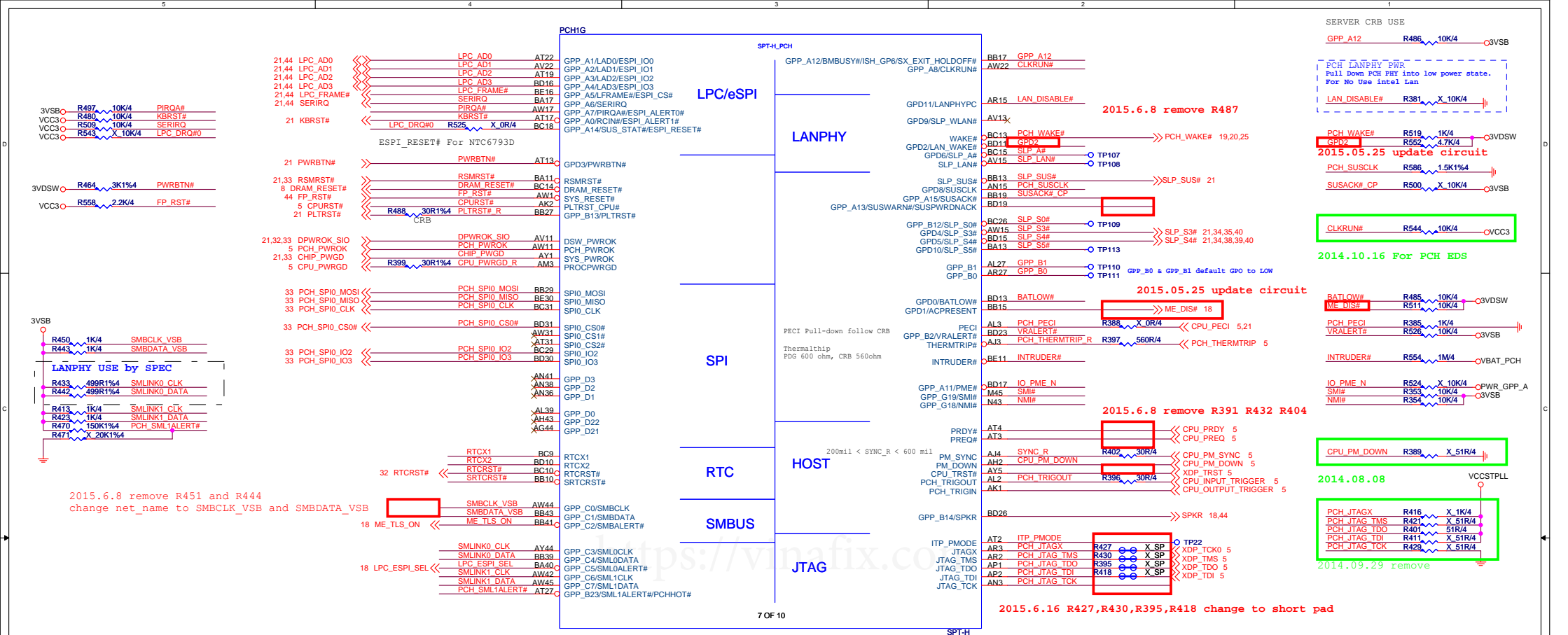


3 OF 10

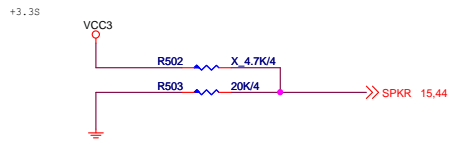
W/ SMI/NMI Funtion

GPP_B[23:20,14]
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]



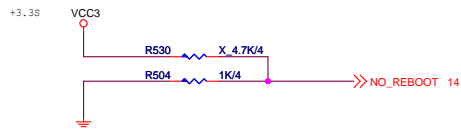


TOP Swap



Internal pull-down 20K is disabled after PLTRST#

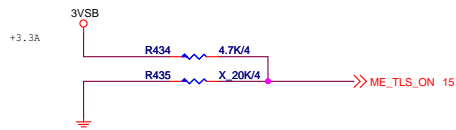
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

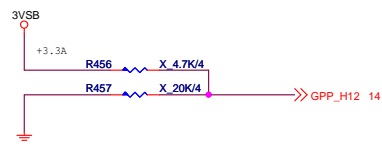
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

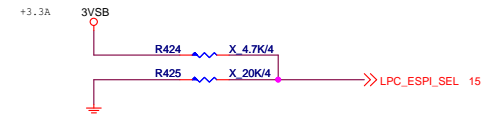
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

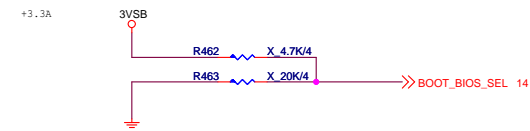
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

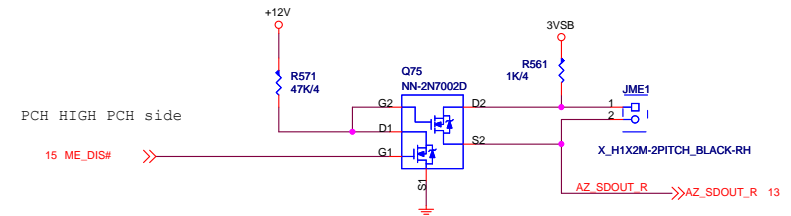
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

HDA_SDO



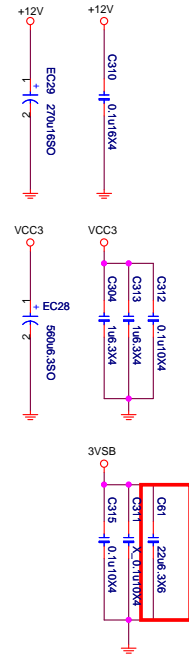
MICRO-STAR INT'L CO.,LTD

MS-7996

Size	Document Description	Rev
Custom	PCH-Strap	12
Date: Wednesday, September 23, 2015	Sheet 18 of 51	

2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB

15,20,38 SMBCLK_VSB
15,20,38 SMBDATA_VSB



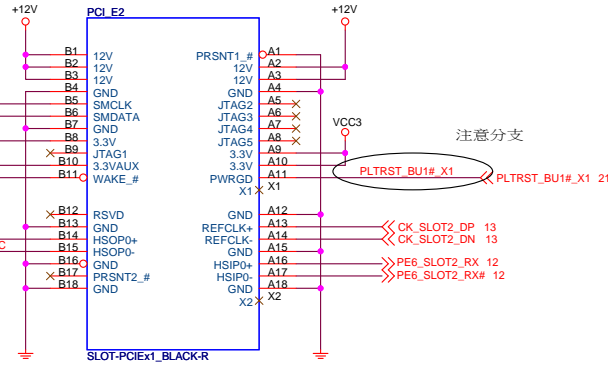
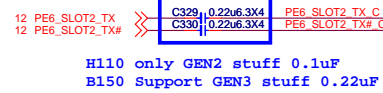
2015.6.16 add C61



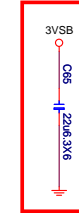
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB



2014.12.29



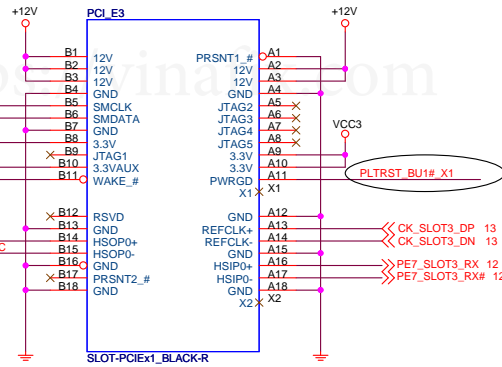
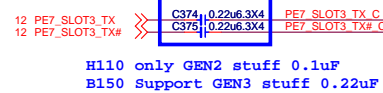
2015.6.16 add C65



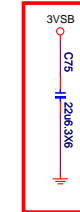
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB



2014.12.29



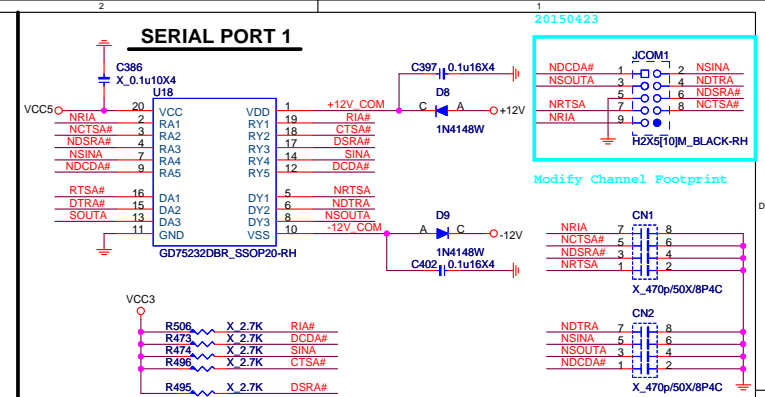
2015.6.16 add C75



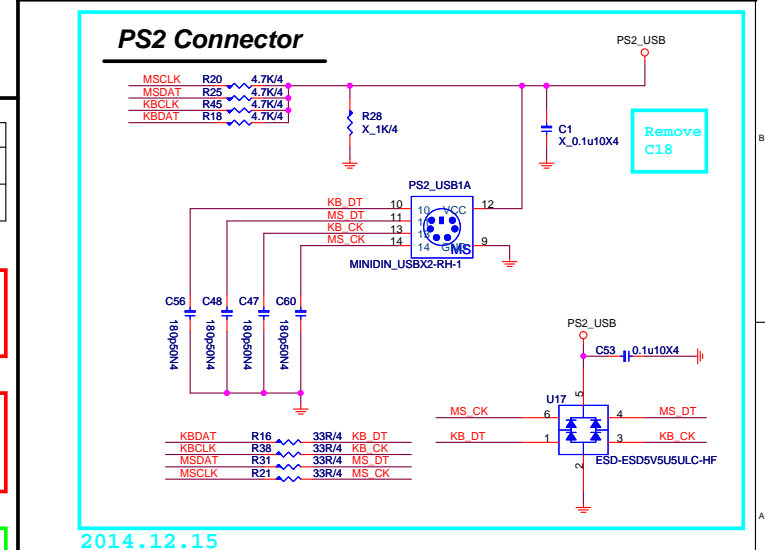
MICRO-STAR INT'L CO.,LTD

MS-7996

Size	Document Description	Rev
Custom	PCIE SLOT-PCH(X1)	12
Date: Wednesday, September 23, 2015	Sheet 20 of 51	



PIN	5563D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	24M_48M_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE
21	TESTMODE1_EN	SOUTA	DISABLE TESTMODE	ENABLE TESTMODE

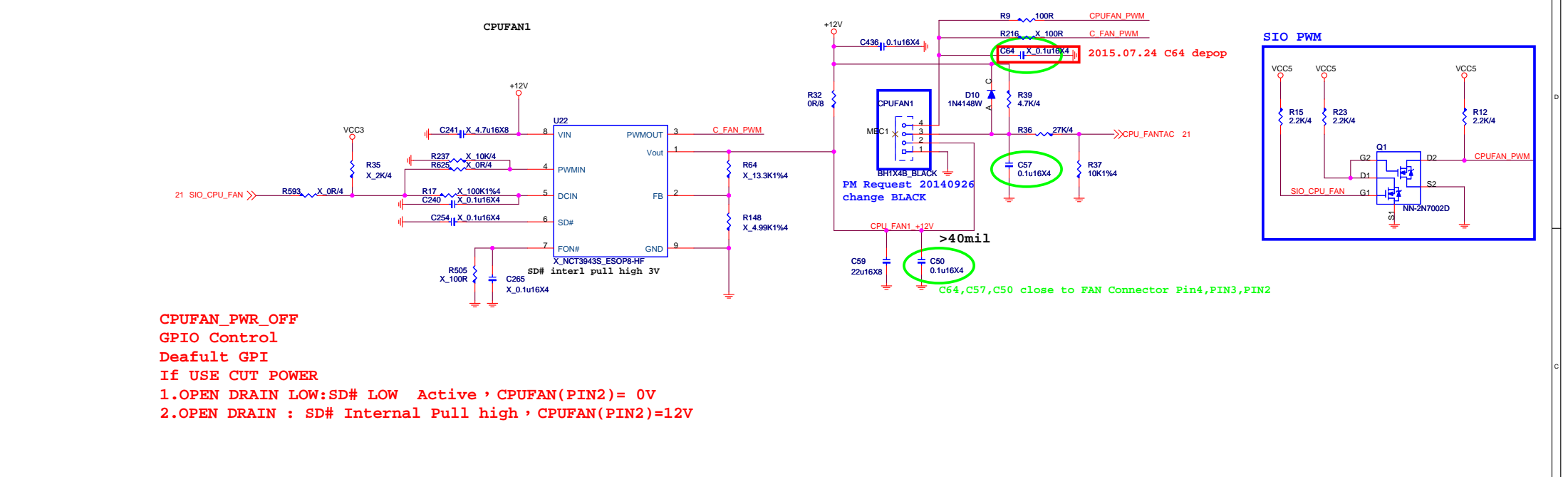


2014.12.15

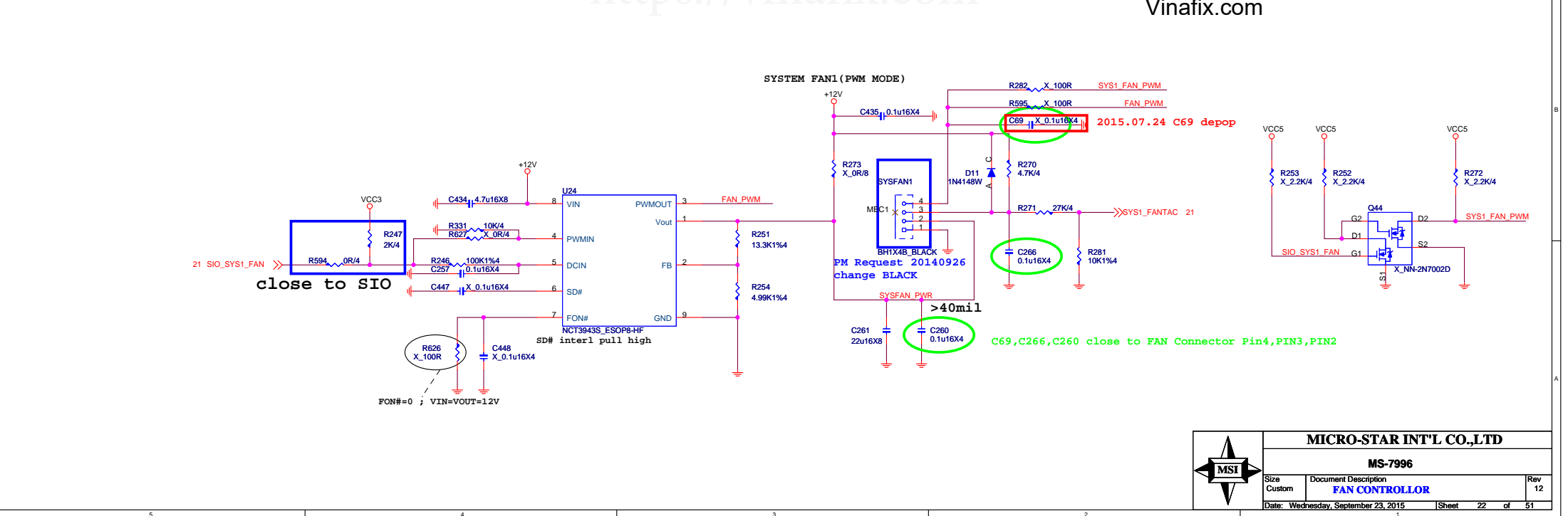


Size Custom	Document Description SIO-NCT5563D-M	Rev 12
Date: Wednesday, September 23, 2015		Sheet 21 of 51

Type G : 4 PIN CPU FAN FROM SIO



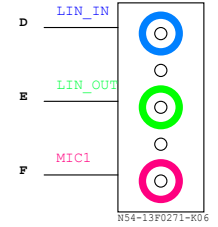
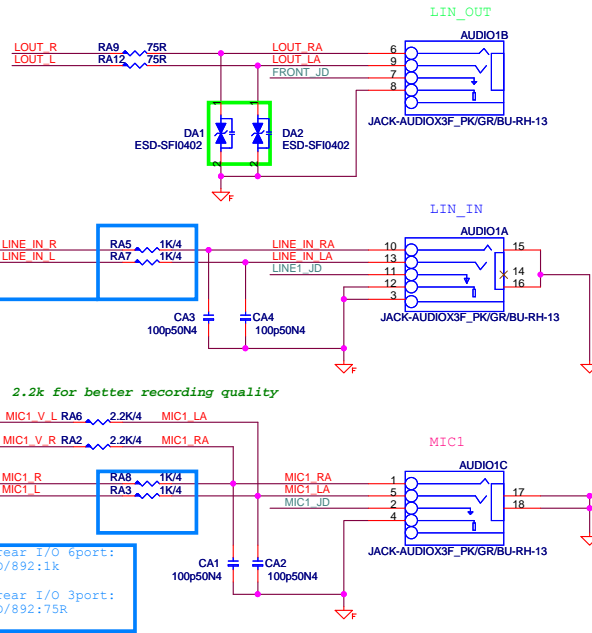
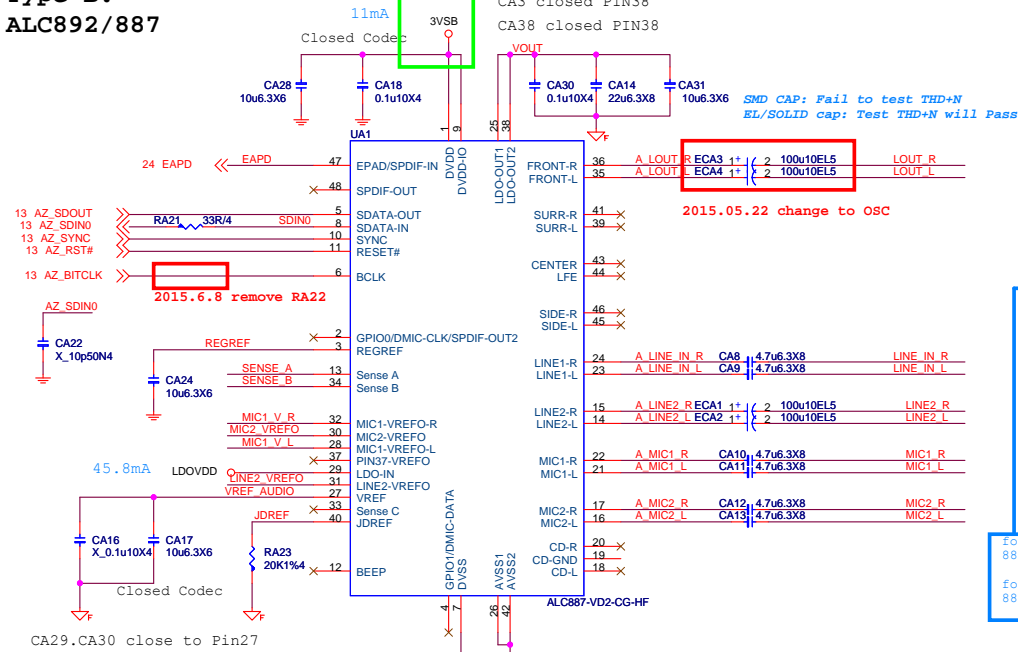
Type H : 4 PIN SYS FAN FROM SIO



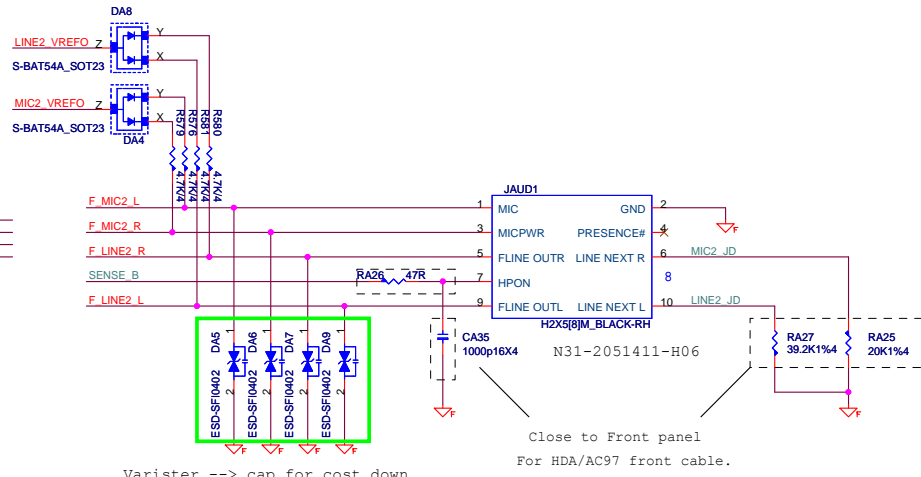
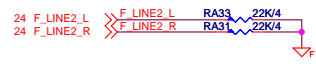
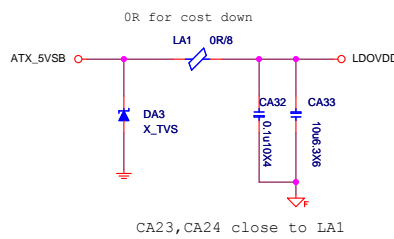
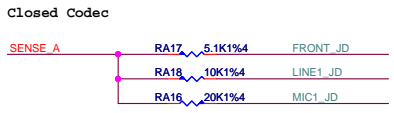
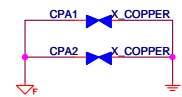
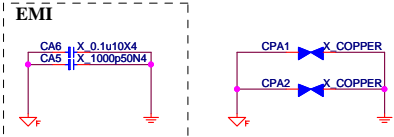
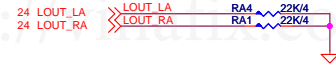
Type B: ALC892/887

2014.09.15

CA4 closed PIN25
CA3 closed PIN38
CA38 closed PIN38



<https://www.aliexpress.com>

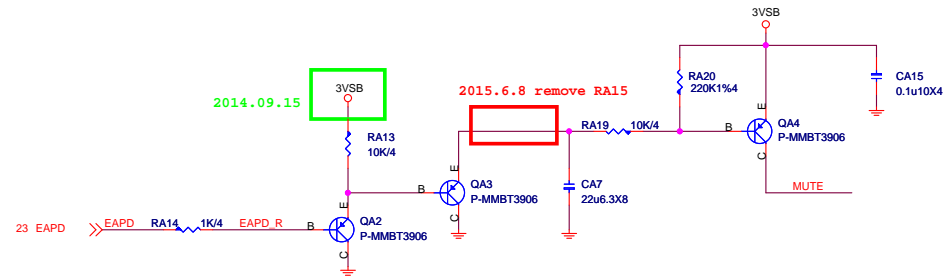


Varistor --> cap for cost down
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack

MICRO-STAR INT'L CO.,LTD			
MS-7996			
Size	Document Description	Rev	
Custom	AUDIO - ALC892/887	12	
Date: Wednesday, September 23, 2015	Sheet 23 of 51		

Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



<https://vinafix.com>

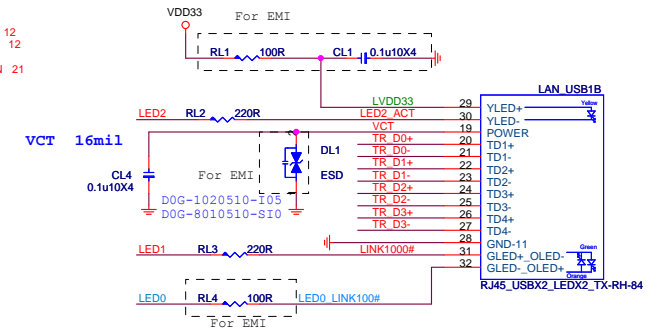
History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

LAN Connector



Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

<https://vinafix.com>

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

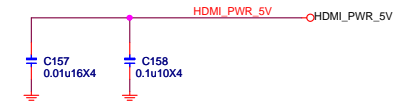
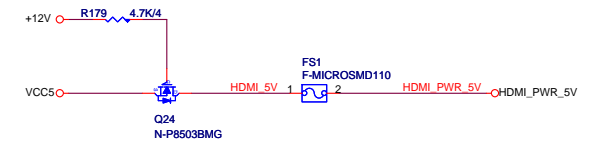
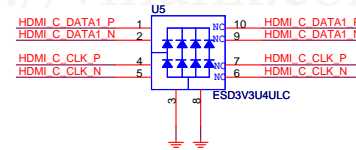
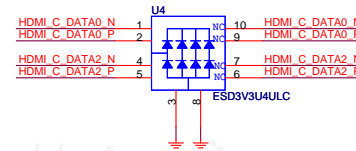
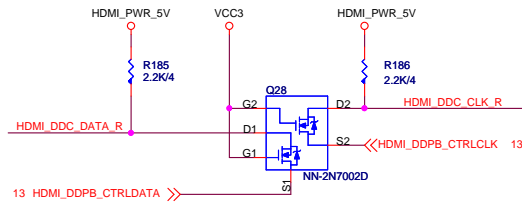
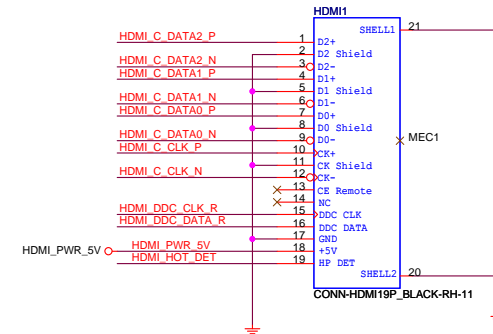
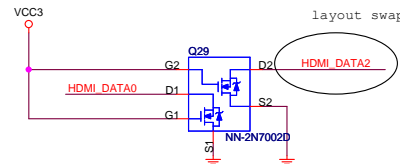
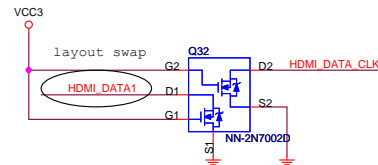
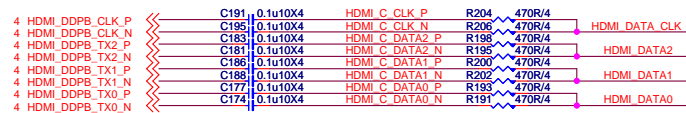


MICRO-STAR INT'L CO.,LTD

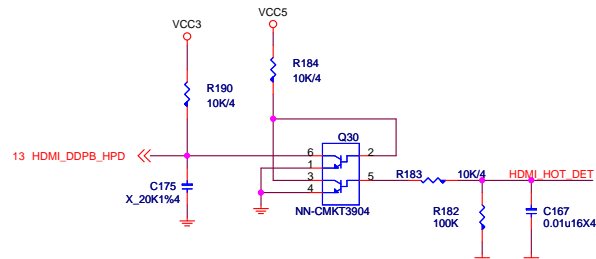
MS-7996

Size	Document Description	Rev
Custom	LAN - RTL8111H	12
Date: Wednesday, September 23, 2015	Sheet 25 of 51	

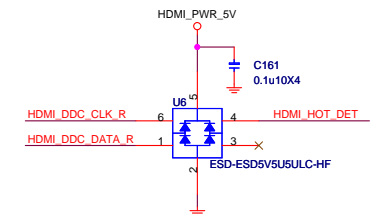
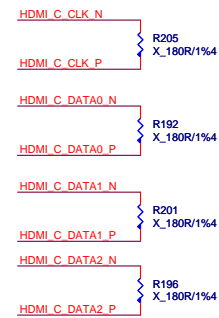
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



HPD

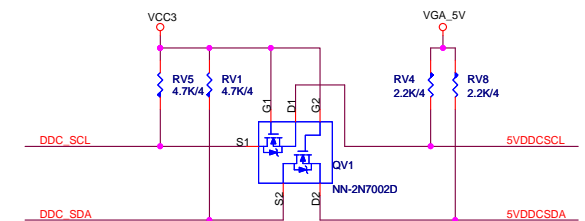
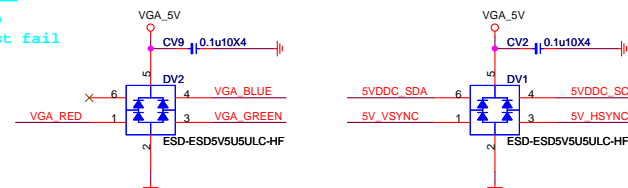
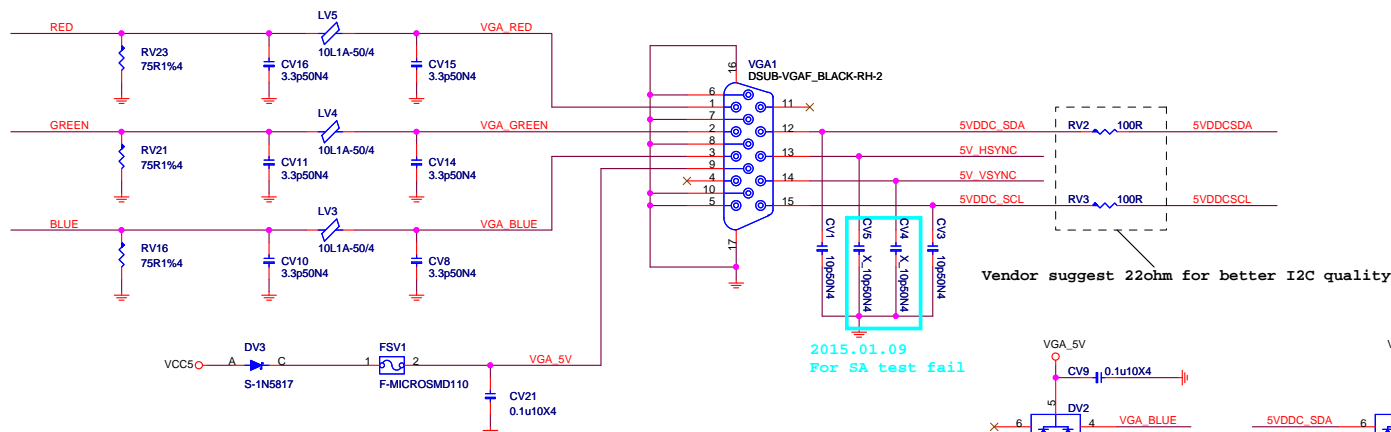
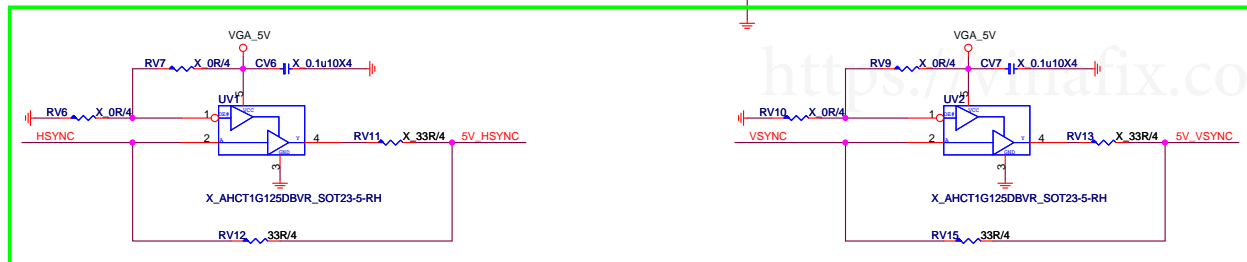
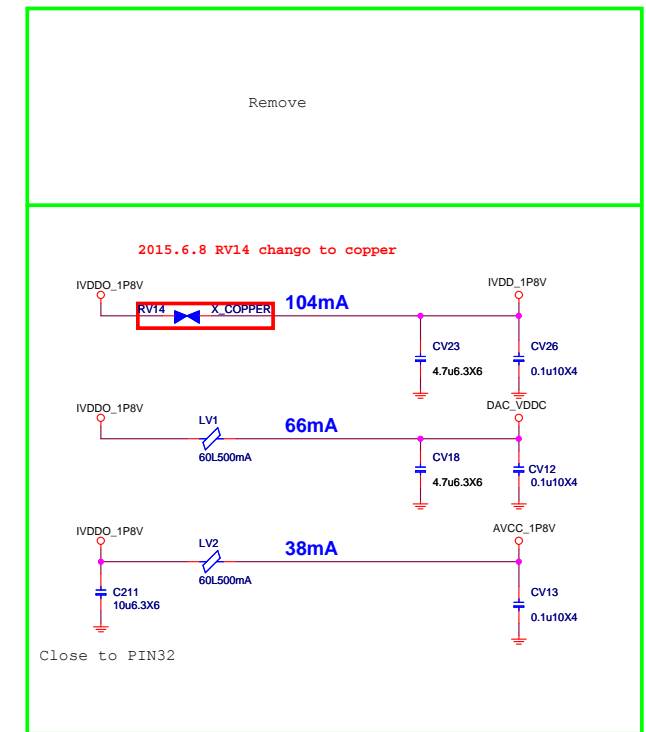
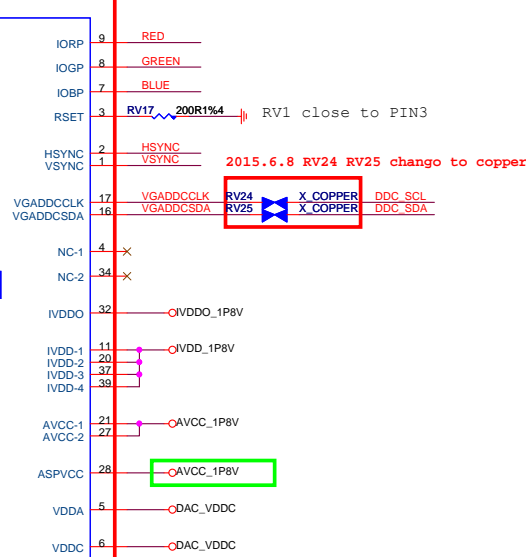


For EMI



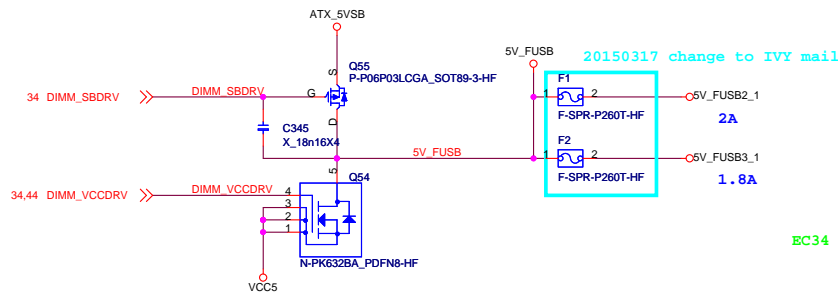
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

						UV3	
4	DP_DDPO_TXP0	CV22	0.1u10x4	DP_DDPO_TXP0	22		
4	DP_DDPO_TXN0	CV20	0.1u10x4	DP_DDPO_TXN0	23		RX0P RX0N
Differential impedance = 100 ohm							
4	DP_DDPO_TXP1	CV19	0.1u10x4	DP_DDPO_TXP1	25		
4	DP_DDPO_TXN1	CV17	0.1u10x4	DP_DDPO_TXN1	26		RX1P RX1N
4	DP_AUXP	CV25	0.1u10x4	DP_AUXP	19		
4	DP_AUXN	CV24	0.1u10x4	DP_AUXN	18		RXAUXP RXAUXN

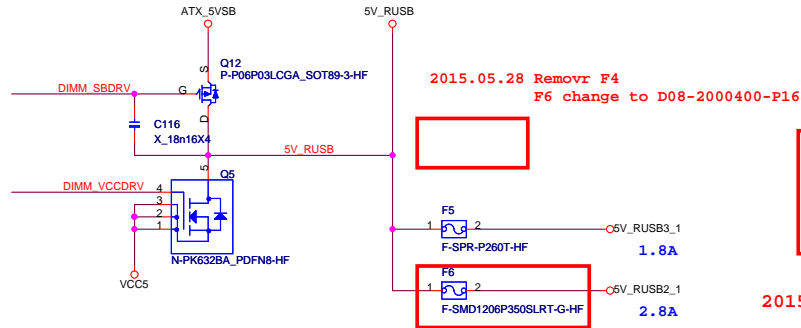


MS-7996

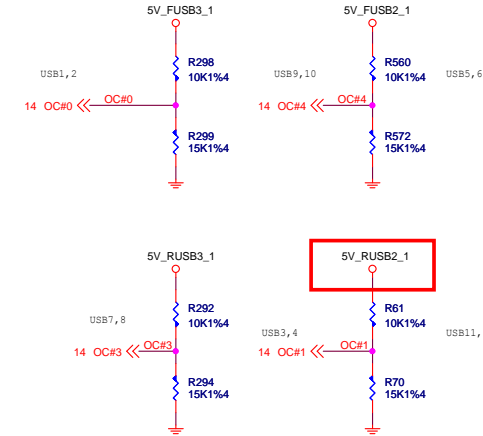
Size Custom	Document Description VGA - ITE6515	Rev 12
Date: Wednesday, September 23, 2015		Sheet 28 of 51



2015.05.28 Remove USB CAP EC33

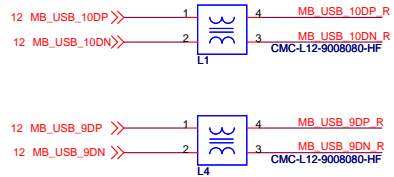


2015.05.28 Remove USB CAP EC3

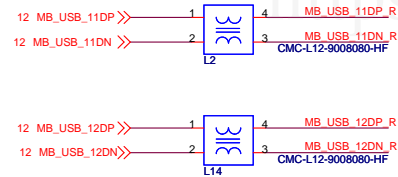


2015.05.28 change to 5V_RUSB2_1
2015.06.08 Remove R559,R575 and R605,R409

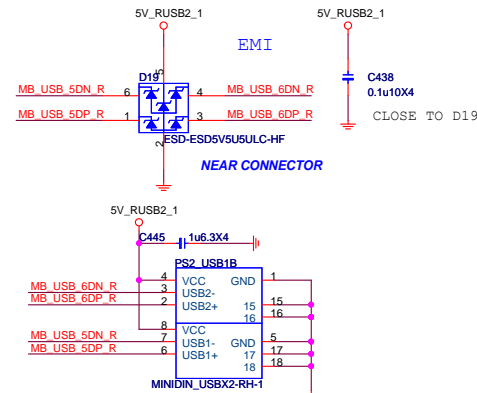
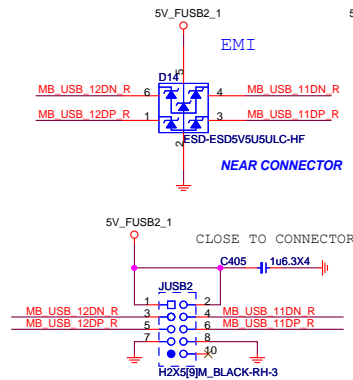
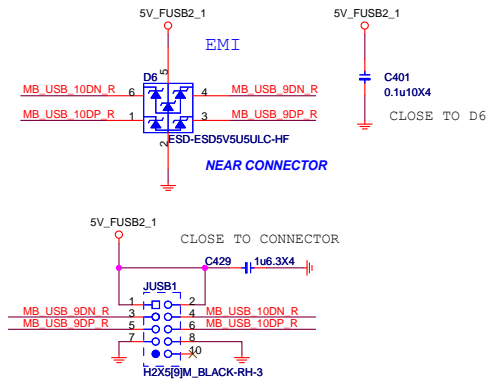
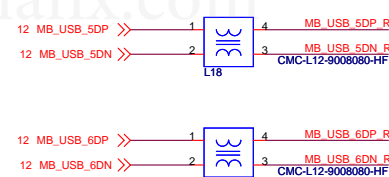
FRONT USB PORT 9,10



FRONT USB PORT 11,12



REAR USB PORT 5,6



2015.05.22 JUSB2 change to USB11,12
PS2_USB change to USB5,6

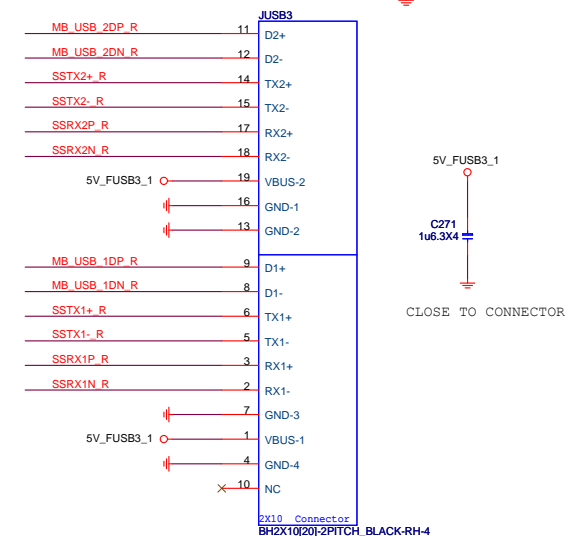
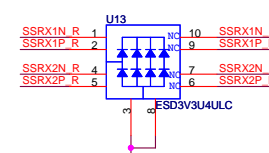
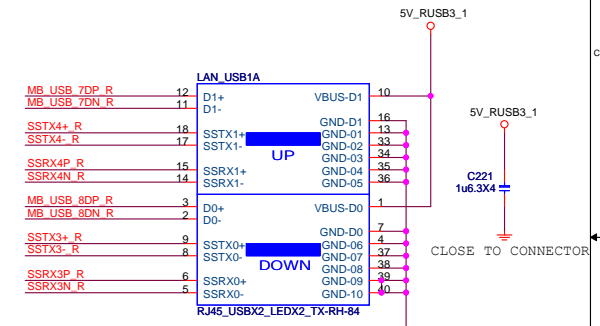
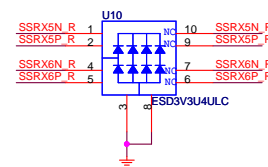
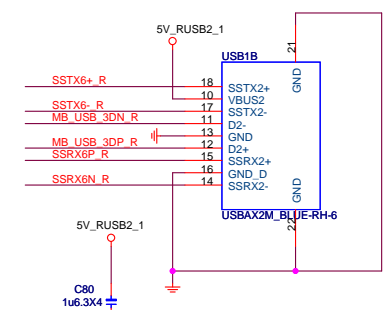
Vinafix.com

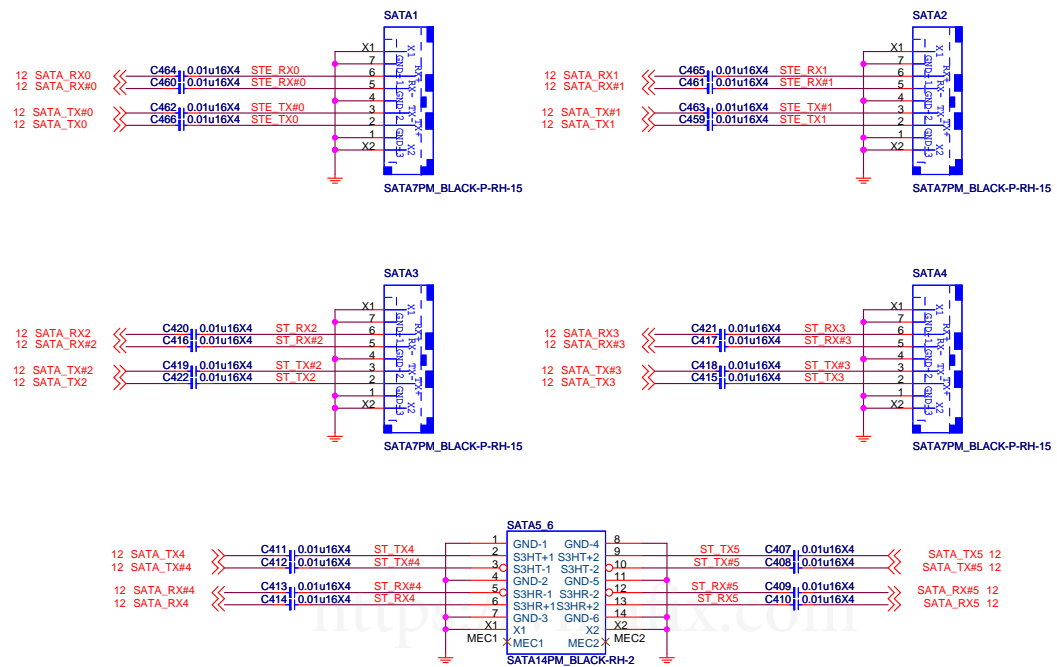


MICRO-STAR INT'L CO.,LTD

MS-7996

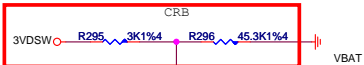
Size	Document Description	Rev
Custom	USB2.0 Connector	12
Date: Wednesday, September 23, 2015	Sheet 29 of 51	





CUT_VBAT

2015.7.20 R295,R296 change to POP

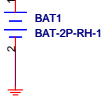


Close to PCH

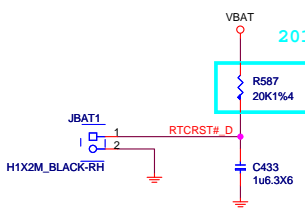
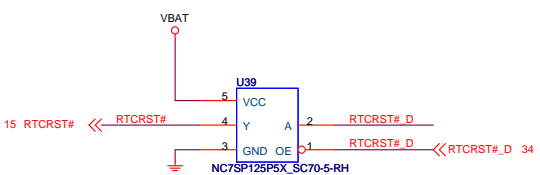


2015.6.1 add VBAT1 in bottom side

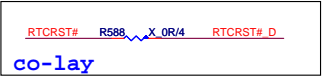
R287 1K1%4



tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

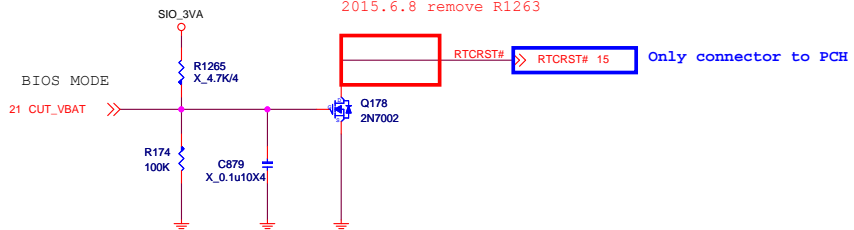


2014.12.29

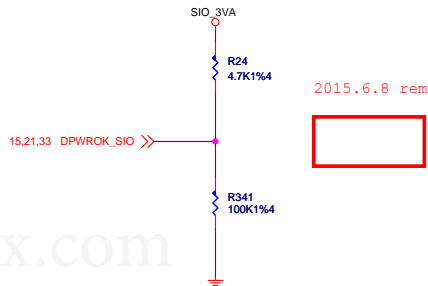


Vinafix.com

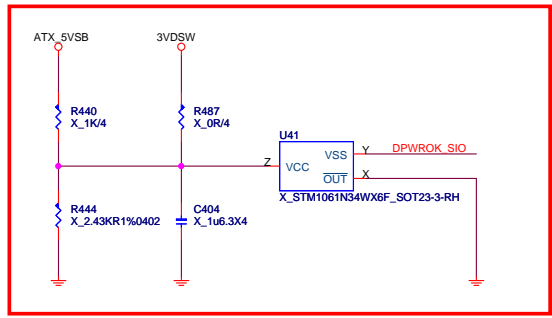
2015.6.8 remove R1263



2015.6.8 remove R342



2015.6.10 add circuit



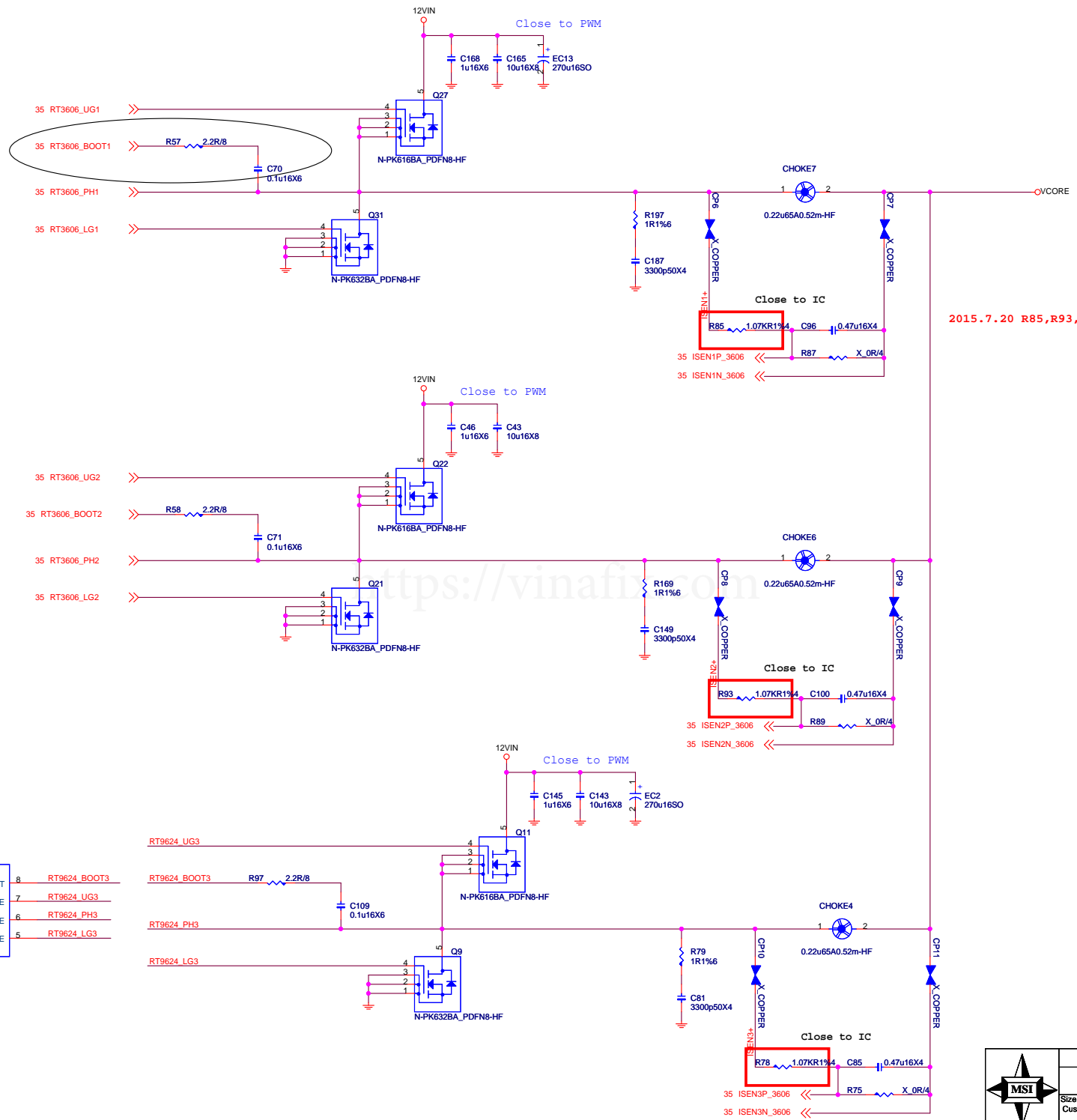
MICRO-STAR INT'L CO.,LTD

MS-7996

Size	Document Description	Rev
Custom	CUT_VABT circuit	12
Date:	Wednesday, September 23, 2015	Sheet 32 of 51

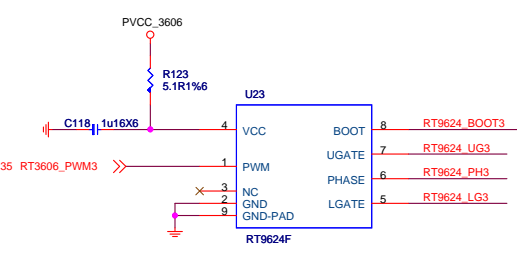
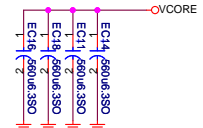


D03-0341409-A68 / D03-0230019-A30

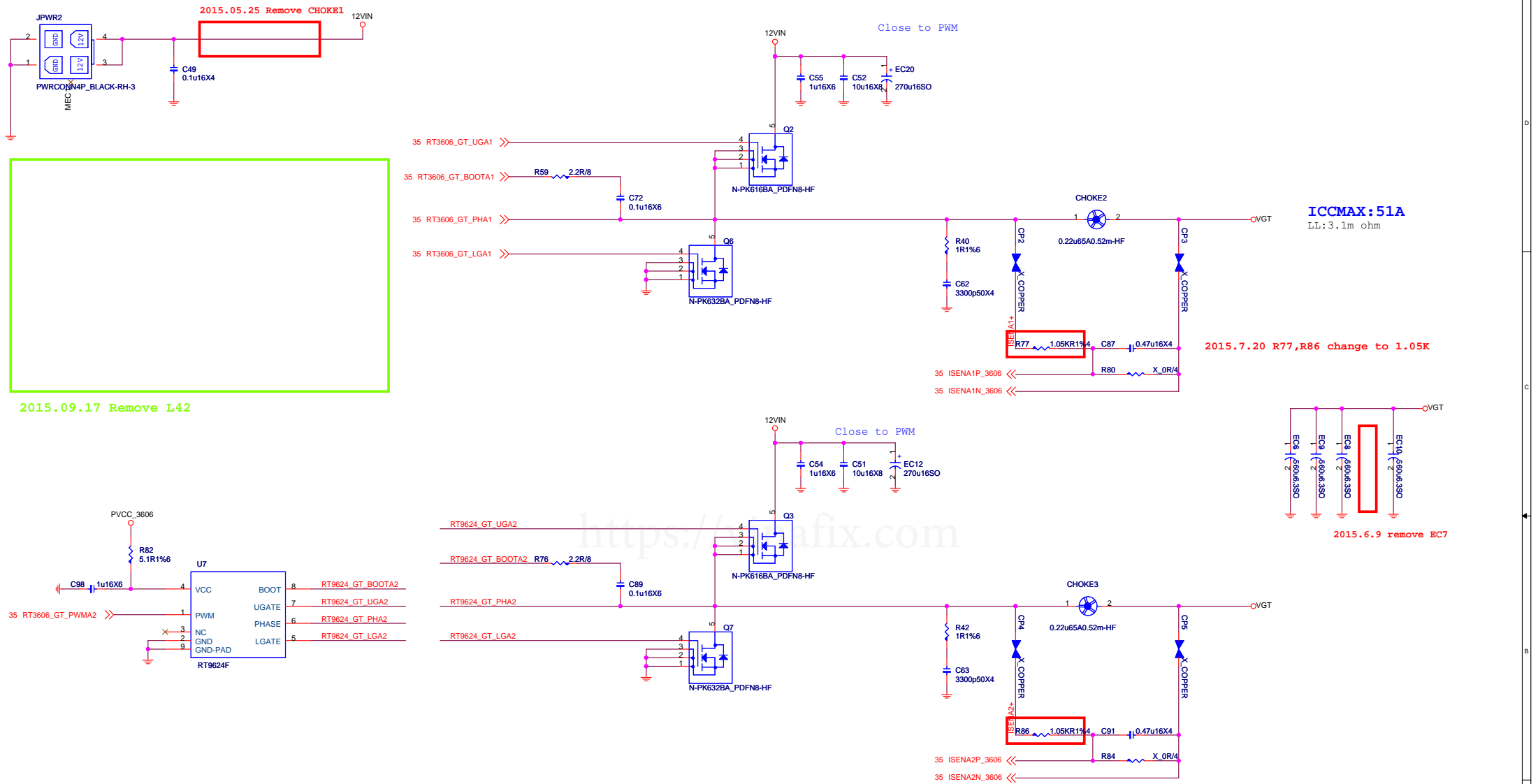


ICCMAX: 79A
LL: 2.1m ohm

2015.7.20 R85,R93,R78 change to 1.07K



MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size	Document Description	Rev
Custom	VCORE(P-PAK) PHASE1-3	12
Date:	Wednesday, September 23, 2015	Sheet 36 of 51



ICCMAX:51A
LL:3.1m ohm

2015.7.20 R77,R86 change to 1.05K

2015.6.9 remove EC7



MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description VGT(P-PAK) PHASE1-2	Rev 12
Date: Wednesday, September 23, 2015 Sheet 37 of 51		

DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

2.8A FOR CPU

4.8A FOR 2DIMM DDR4

0.375A FOR VTT_DDR

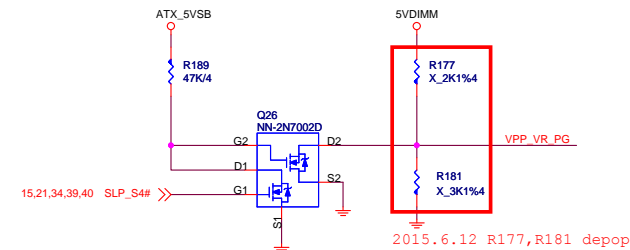
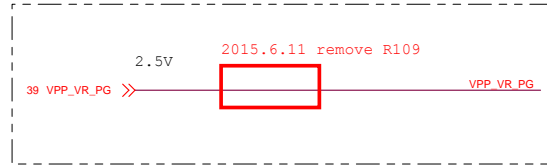
OCP = 7.925A*1.5=11.8875A

Current limit= 95.3K(R1054)*5uA/10/4mohm)=11.91A

2015.05.22 change to DDR4

VID	Reference Voltage (V)
H	0.675
L	0.75

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))} \\ &= 9.357 * 0.44 \\ &= 4.154A \end{aligned}$$

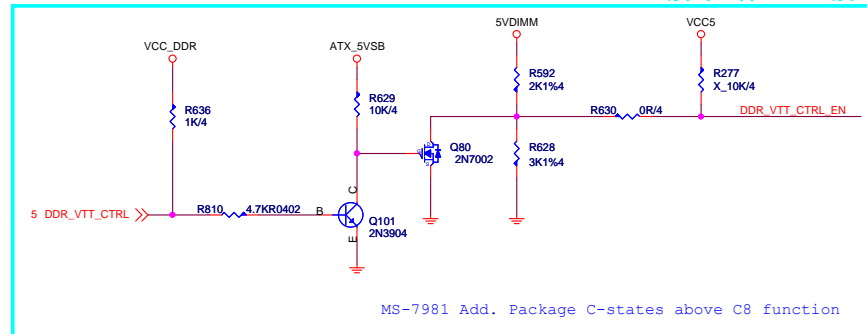


2015.6.11 remove circuit



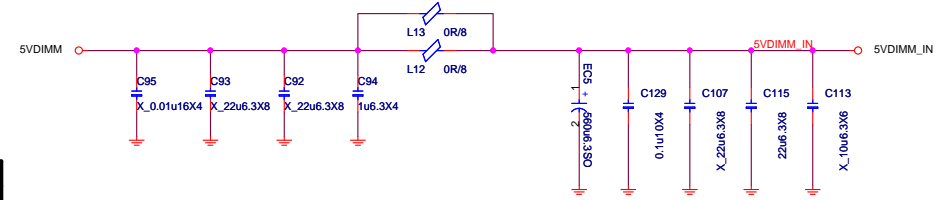
SLP_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down



MS-7981 Add. Package C-states above C8 function

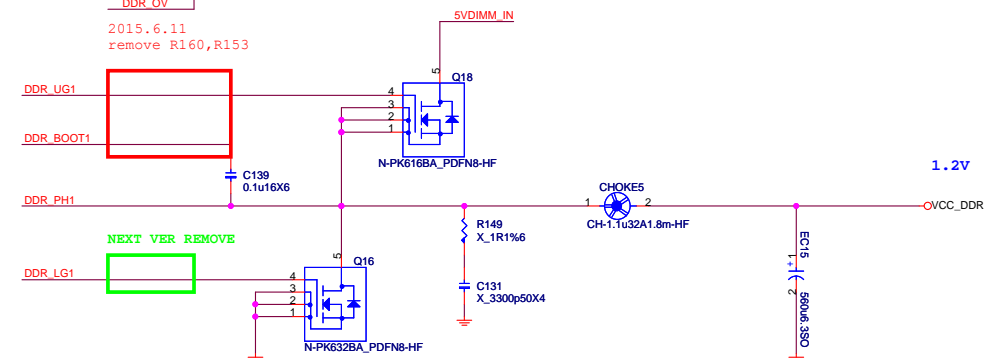
MS-7981 change to using RT8231



By layout modify

MAX: 7.925A

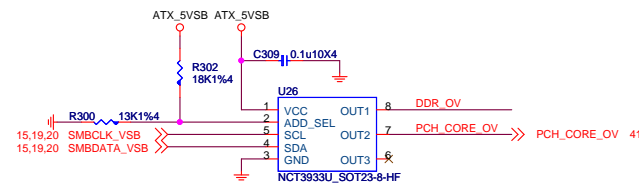
1.2V



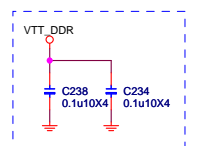
1.2V

UPI VOLTAGE CONSOLE

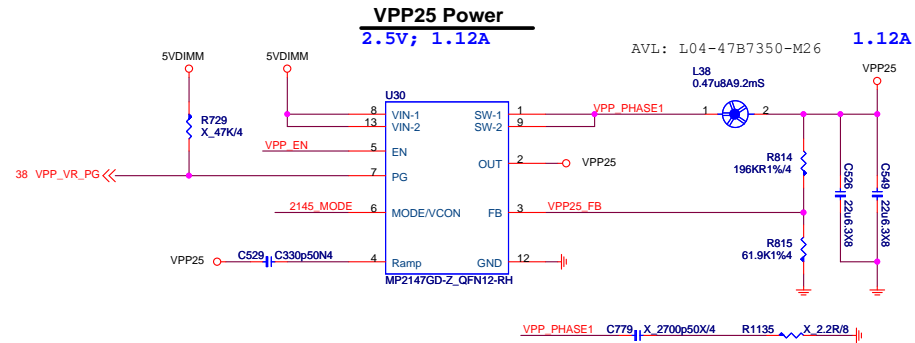
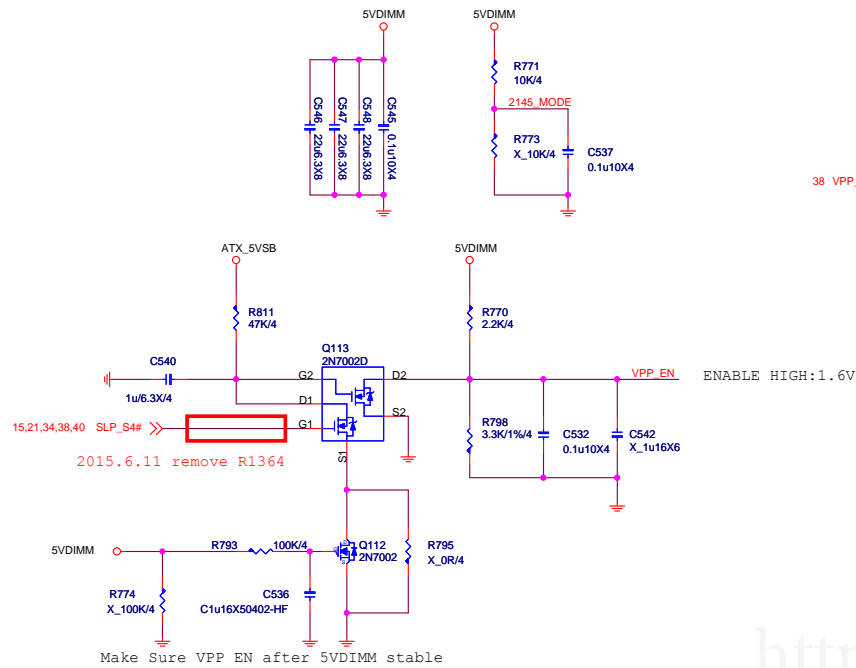
0x26: RH=18K, RL=13K



0.1uFx1 per dimm



2DIMM :1.12A FOR DDR VPP2.5V



MICRO-STAR INT'L CO.,LTD

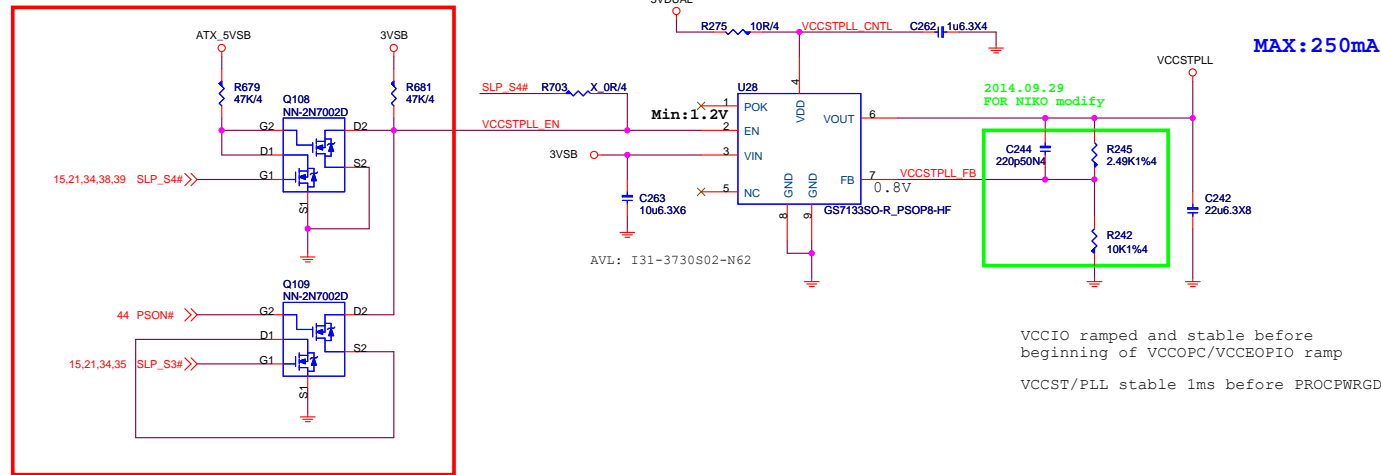
MS-7996

Size Custom	Document Description DDR-MP2147-VPP25	Rev 12
Date: Wednesday, September 23, 2015		Sheet 39 of 51

VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge



2015.05.25 add circuit

<https://vinafix.com>

1.0V; 7.858A

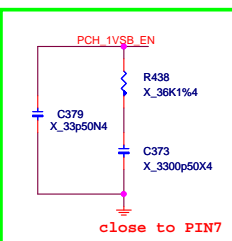
Rocs:5.9K,OCP:
D03-4C05N03-O05 : 11.8A
D03-632BA0C-N03 : 12.82A
use UBIQ MOS need Check

Rdson(1ow)4.5V

D03-4C05N03-O05	: 5 mohm
D03-632BA0C-N03	: 4.6mohm
D03-3056M00-U47	: 6.2mohm

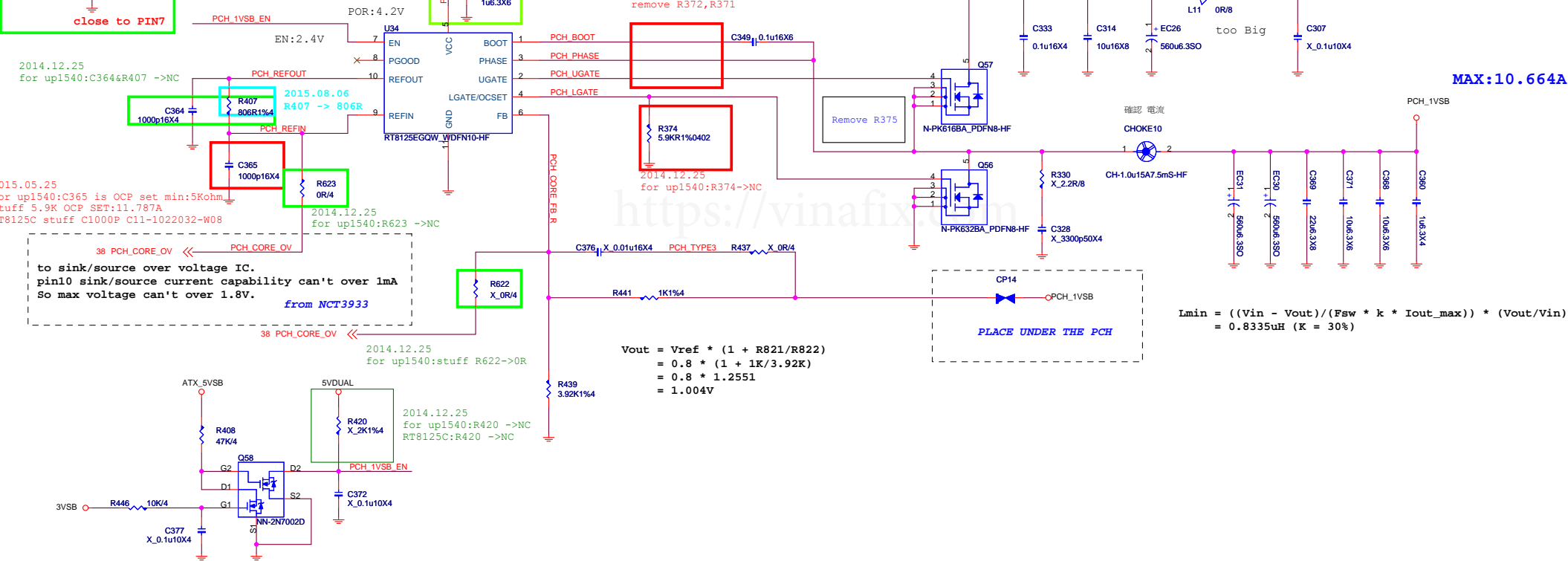
2015.04.23 change to UP1540

2014.08.22 close to U34



```
2015.01.22
for up1540:stuff R438->36K,
C379->NC,C373->3.3nF
for RT8125:R438.C379.C373->NC
```

```
2015.01.22
for up1540:R403->2.2R,C362->1uF
for RT8125:R403->10R,C362->1uF
```

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))} \\ &= 10.664 * 0.4 \\ &= 4.2656A < 5000mA \end{aligned}$$


MAX:10.664A

$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$

$$= 0.8335 \mu H \text{ (K = 30\%)}$$
$$\begin{aligned} V_{out} &= V_{ref} * (1 + R_{821}/R_{822}) \\ &= 0.8 * (1 + 1K/3.92K) \\ &= 0.8 * 1.2551 \\ &= 1.004V \end{aligned}$$

PLACE UNDER THE PCH



MICRO-STAR INT'L CO.,LTD

MS-7996

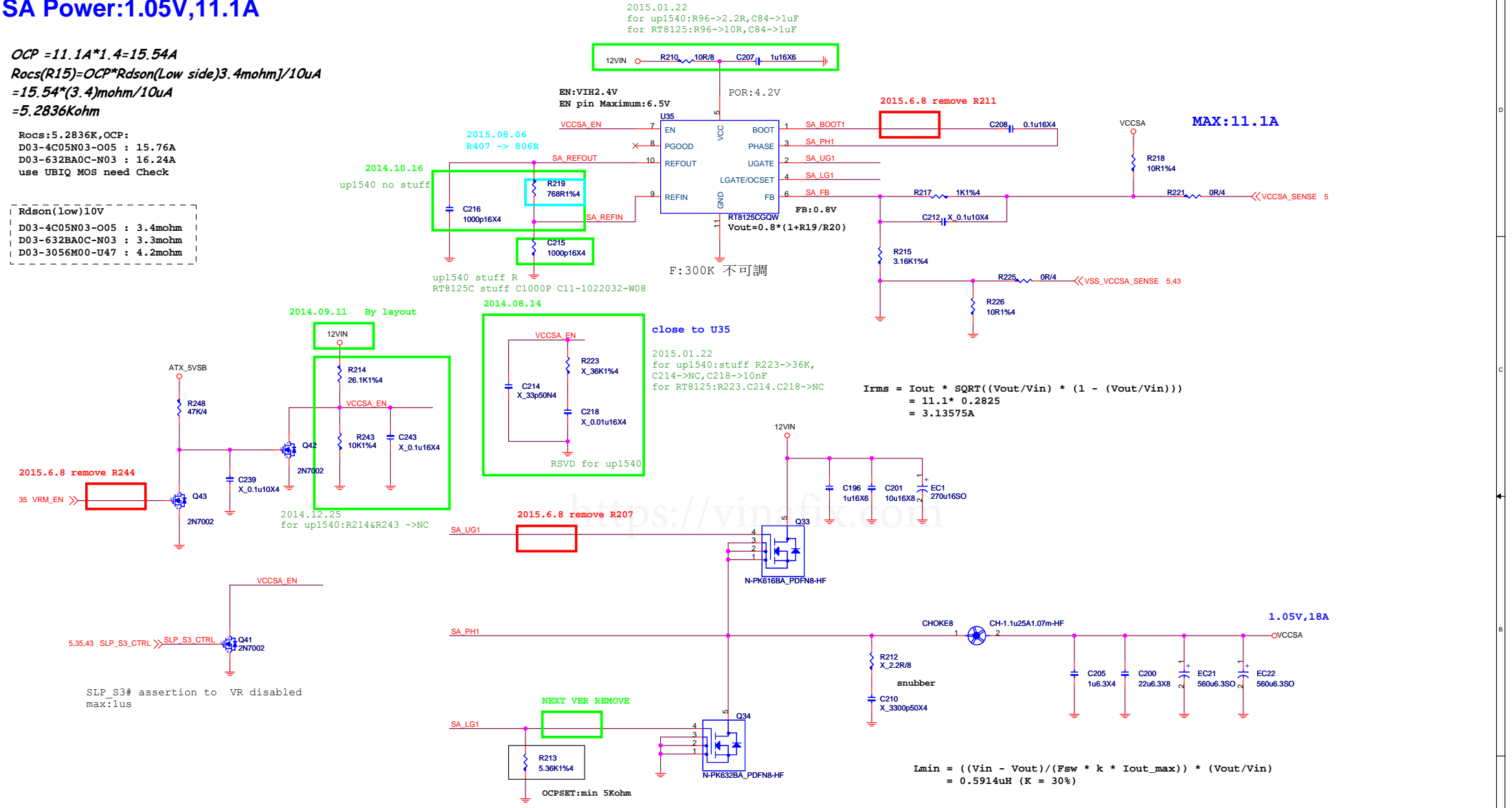
Size Custom	Document Description PCH Core power	Rev 12
Date: Wednesday, September 23, 2015		Sheet 41 of 51

SA Power:1.05V,11.1A

$OCP = 11.1A * 1.4 = 15.54A$
 $R_{ocs}(R15) = OCP * R_{dson}(Low\ side) / 10uA$
 $= 15.54 * (3.4)mohm / 10uA$
 $= 5.2836Kohm$

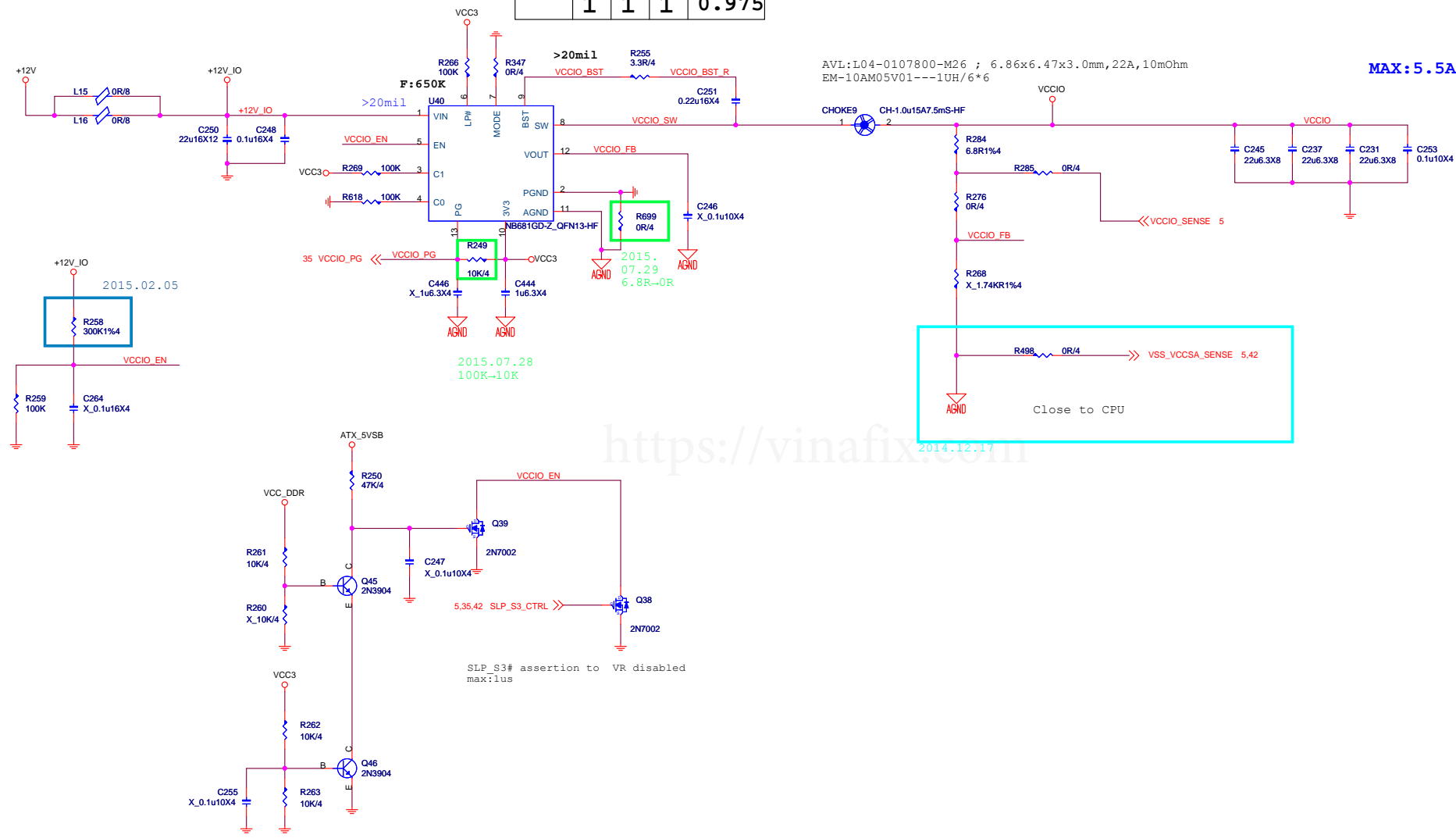
RocS:5.2836K,OCP:
D03-4C05N03-005 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(10V)10V
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm



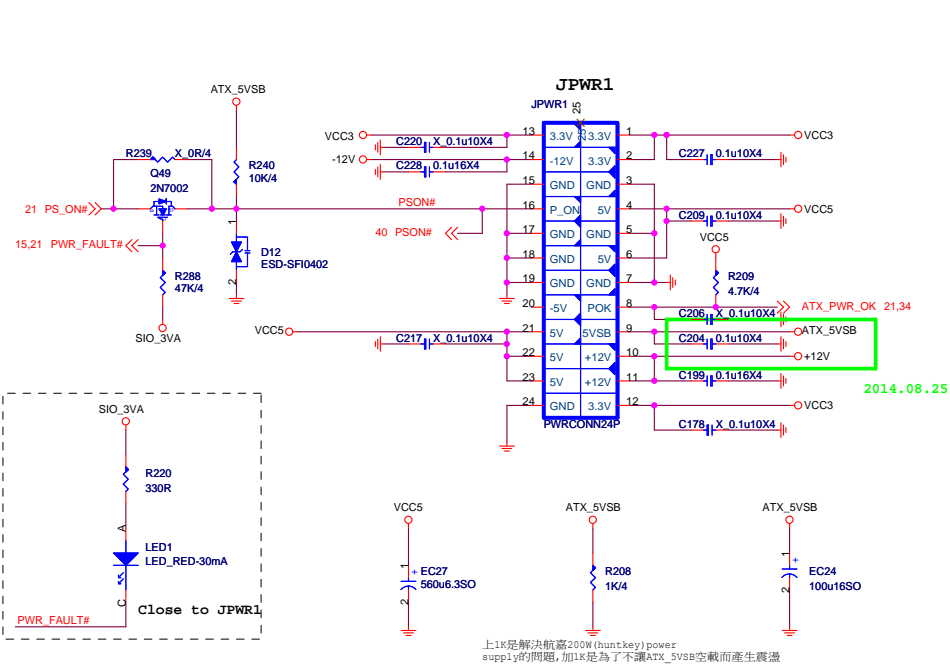
VCCIO
0.95V; 5.5A
IMAX 6A
ILIMIT=8.5~9A

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

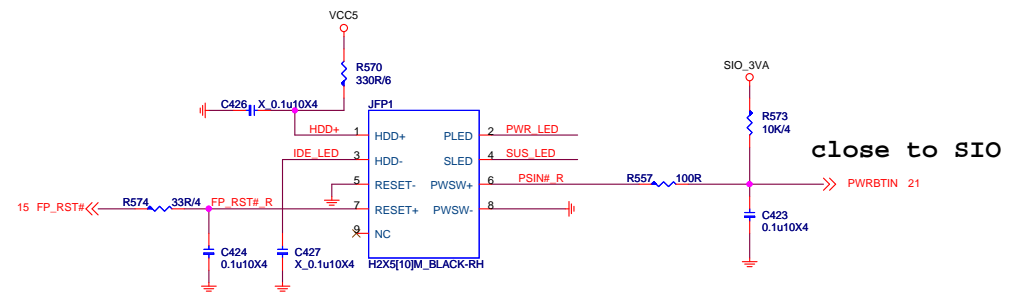


https://vinafix.com

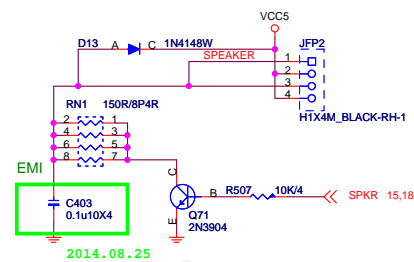
ATX POWER CONNECTOR



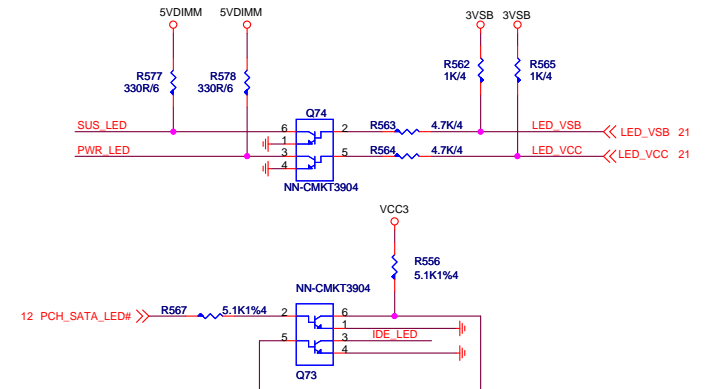
FRONT PANNEL



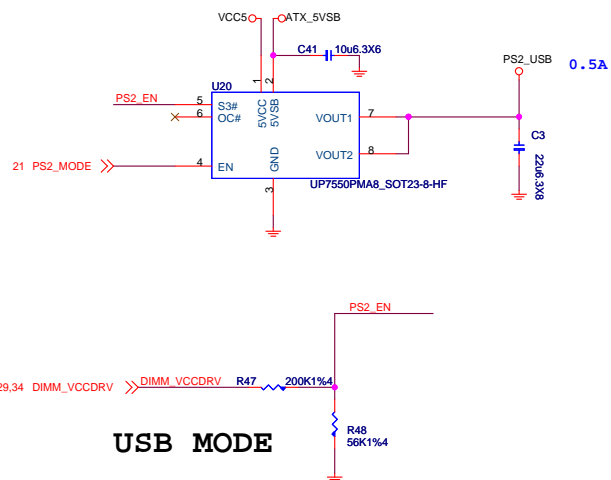
Speaker Pin Header



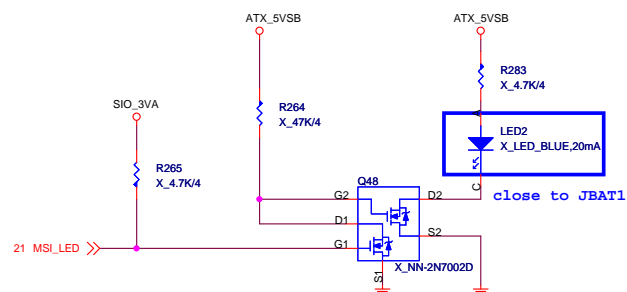
LED (for NV5533)



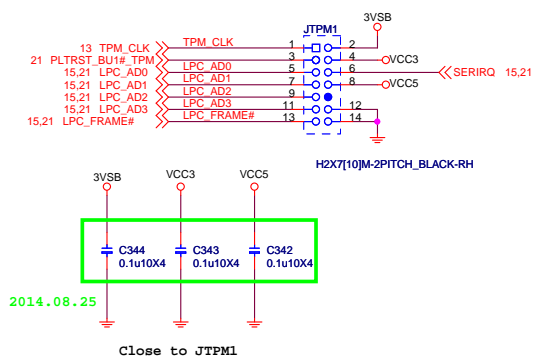
PS2 POWER



MSI LED



TPM

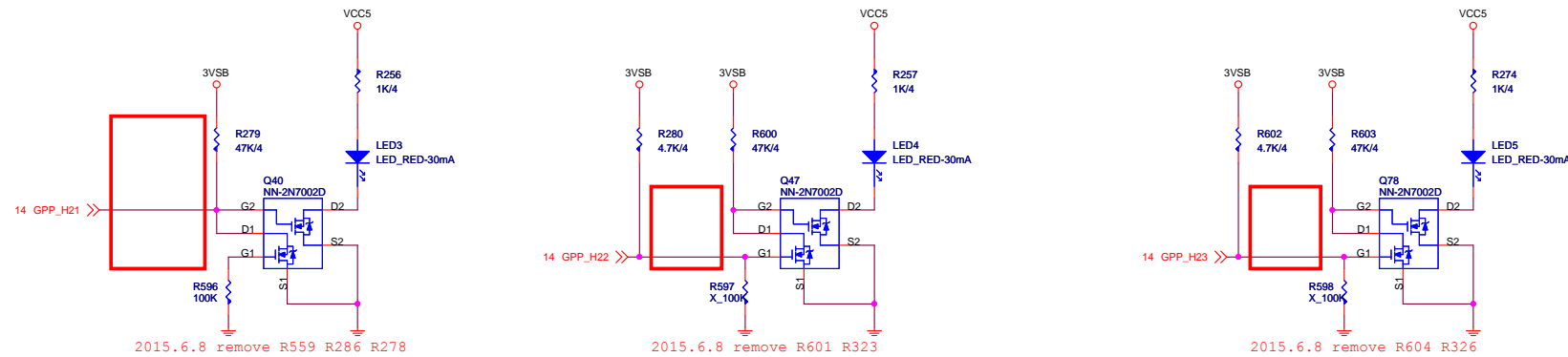


MICRO-STAR INT'L CO.,LTD

MS-7996

Size Custom	Document Description ATX F_Panel/TPM/MSI_LED	Rev 12
Date: Wednesday, September 23, 2015		Sheet 44 of 51

DEBUG LED

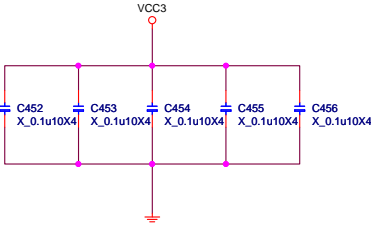
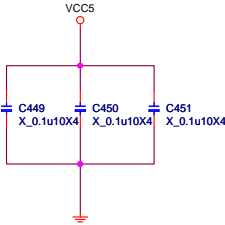


GPIO LED	GPP_H21	GPP_H21	GPP_H21
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

關機斷電狀態下，3個LED先維持default全暗，開機通電後：

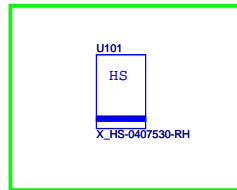
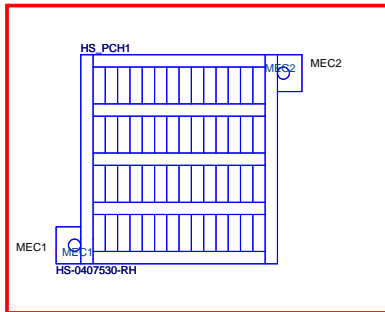
- 1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
- 2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
- 3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
- 4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

EMI CAP

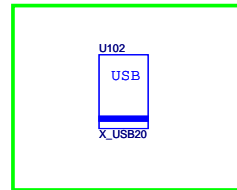


<https://vinafix.com>

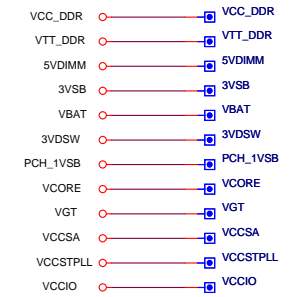
2015.06.01 change to using E31-0407530-K08



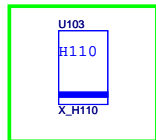
2015.08.03
colay Heatsink for H110



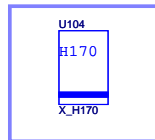
2015.08.03
USB2.0 Connector colay for H110



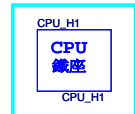
2015.08.03
PCH H110 colay



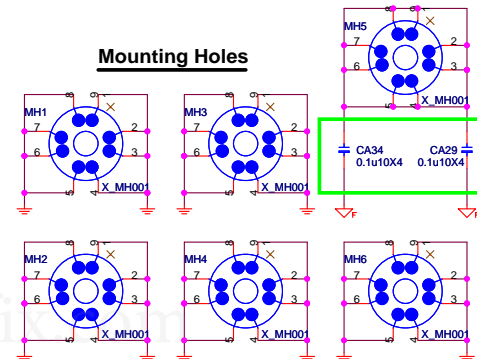
2015.08.10
PCH H110 colay



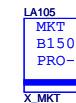
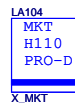
20150423 PM Request cost down



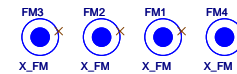
Mounting Holes



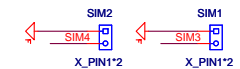
Marketing Name貼紙



Optical Fiducial Marks-120



Simulation



7996_12

2015/09/22 PK0-0799612-E48, 競華, 20, 寶安恩斯邁廠 (MSIS)
2015/09/22 PK0-0799611-G37, 精成-深圳, 21, 寶安恩斯邁廠 (MSIS)